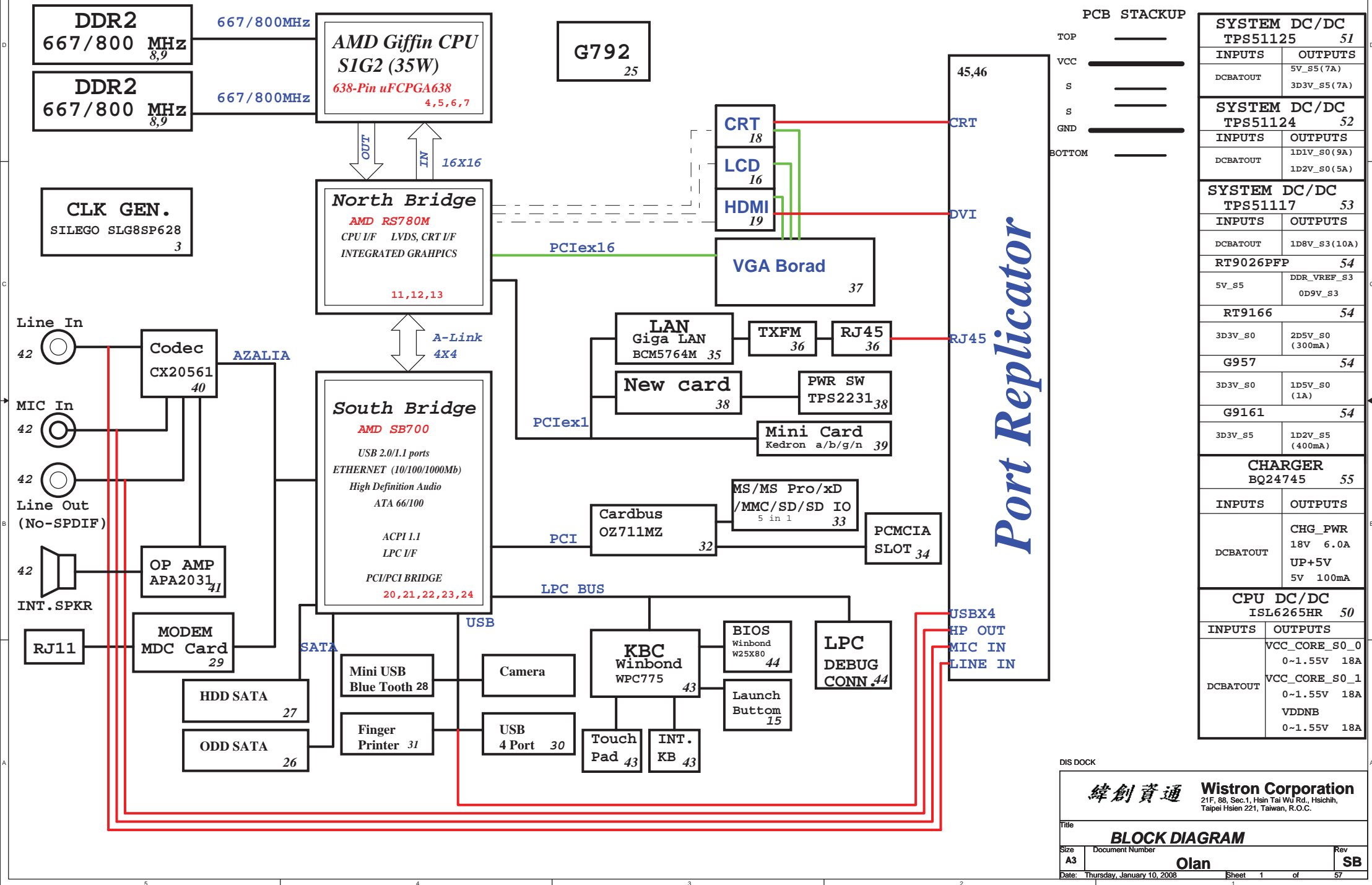


Olan (TM15") Block Diagram

Project code: 91.4Z701.001
PCB P/N : 48.4Z701.0SB
REVISION : 07249-SB



DIS DOCK

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Title

BLOCK DIAGRAM

Size

Document Number

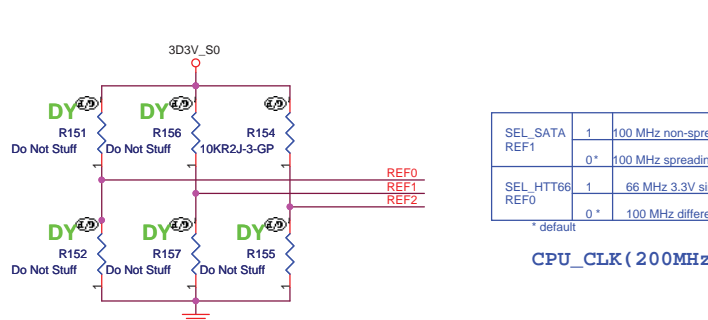
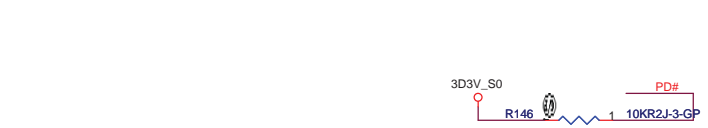
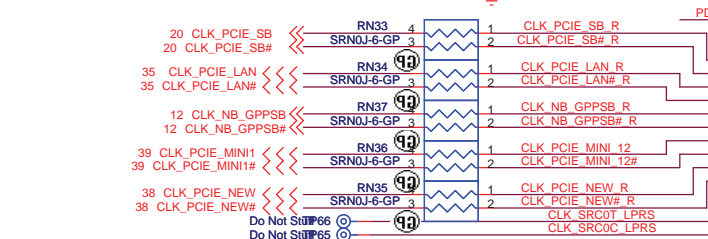
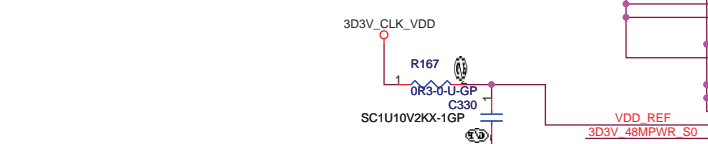
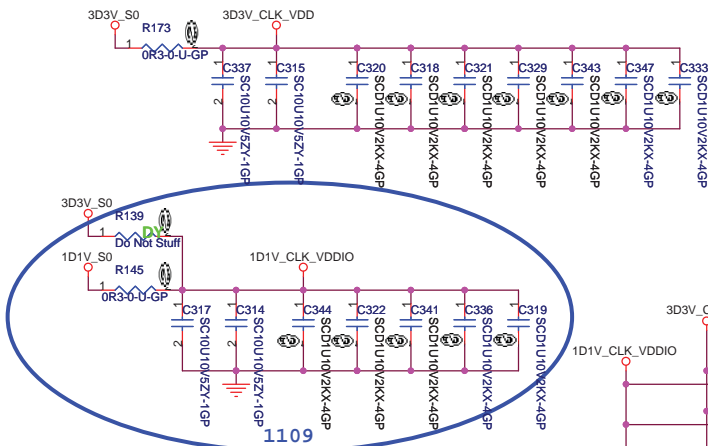
Olan

Rev

SB

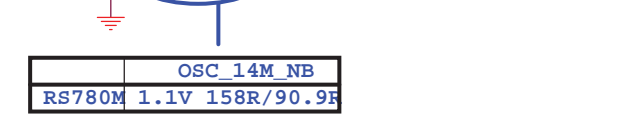
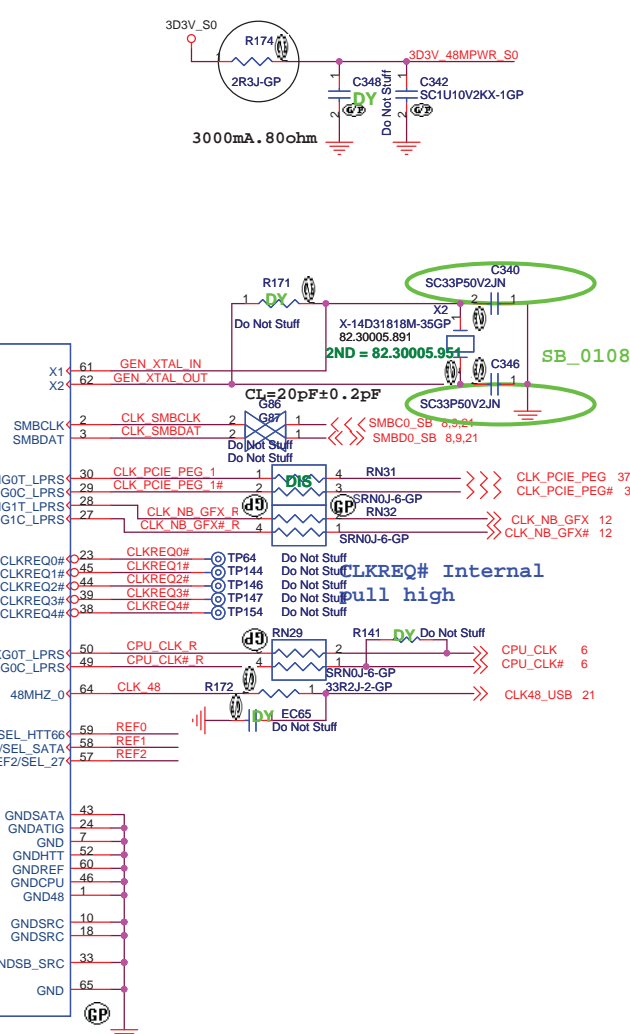
Date: Thursday, January 10, 2008

Sheet 1 of 57



SEL_SATA REF1	1	100 MHz non-spreading differential SRC clock
	0 *	100 MHz spreading differential SRC clock
SEL_HTT66 REF0	1	66 MHz 3.3V single ended HTT clock
	0 *	100 MHz differential HTT clock

* default
CPU_CLK (200MHz)



Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

DIS DOCK

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Title

CLKGEN_ICS9LPRS480

Size A3

Document Number

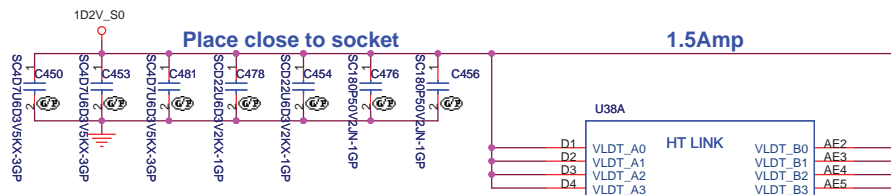
Olan

Rev SA

Date: Thursday, January 10, 2008

Sheet 3 of 57

OSC 14M NB
RS780M 1.1V 158R/90.9F



11 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	HT_CPU_NB_CAD_H0	11
11 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	HT_CPU_NB_CAD_L0	11
11 HT_NB_CPU_CAD_H1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	HT_CPU_NB_CAD_H1	11
11 HT_NB_CPU_CAD_L1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	HT_CPU_NB_CAD_L1	11
11 HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	HT_CPU_NB_CAD_H2	11
11 HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	HT_CPU_NB_CAD_L2	11
11 HT_NB_CPU_CAD_H3	H1	L0_CADIN_H3	L0_CADOUT_H3	AA2	HT_CPU_NB_CAD_H3	11
11 HT_NB_CPU_CAD_L3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	HT_CPU_NB_CAD_L3	11
11 HT_NB_CPU_CAD_H4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	HT_CPU_NB_CAD_H4	11
11 HT_NB_CPU_CAD_L4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	HT_CPU_NB_CAD_L4	11
11 HT_NB_CPU_CAD_H5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	HT_CPU_NB_CAD_H5	11
11 HT_NB_CPU_CAD_L5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	HT_CPU_NB_CAD_L5	11
11 HT_NB_CPU_CAD_H6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	HT_CPU_NB_CAD_H6	11
11 HT_NB_CPU_CAD_L6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	HT_CPU_NB_CAD_L6	11
11 HT_NB_CPU_CAD_H7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	HT_CPU_NB_CAD_H7	11
11 HT_NB_CPU_CAD_L7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	HT_CPU_NB_CAD_L7	11
11 HT_NB_CPU_CAD_H8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	HT_CPU_NB_CAD_H8	11
11 HT_NB_CPU_CAD_L8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	HT_CPU_NB_CAD_L8	11
11 HT_NB_CPU_CAD_H9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	HT_CPU_NB_CAD_H9	11
11 HT_NB_CPU_CAD_L9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	HT_CPU_NB_CAD_L9	11
11 HT_NB_CPU_CAD_H10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	HT_CPU_NB_CAD_H10	11
11 HT_NB_CPU_CAD_L10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	HT_CPU_NB_CAD_L10	11
11 HT_NB_CPU_CAD_H11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	HT_CPU_NB_CAD_H11	11
11 HT_NB_CPU_CAD_L11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	HT_CPU_NB_CAD_L11	11
11 HT_NB_CPU_CAD_H12	K3	L0_CADIN_H12	L0_CADOUT_H12	V5	HT_CPU_NB_CAD_H12	11
11 HT_NB_CPU_CAD_L12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	HT_CPU_NB_CAD_L12	11
11 HT_NB_CPU_CAD_H13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	HT_CPU_NB_CAD_H13	11
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11 HT_NB_CPU_CAD_H14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	HT_CPU_NB_CAD_H14	11
11 HT_NB_CPU_CAD_L14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	HT_CPU_NB_CAD_L14	11
11 HT_NB_CPU_CAD_H15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	HT_CPU_NB_CAD_H15	11
11 HT_NB_CPU_CAD_L15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	HT_CPU_NB_CAD_L15	11
11 HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	HT_CPU_NB_CLK_H0	11
11 HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	HT_CPU_NB_CLK_L0	11
11 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	HT_CPU_NB_CLK_H1	11
11 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	HT_CPU_NB_CLK_L1	11
11 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	HT_CPU_NB_CTL_H0	11
11 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	HT_CPU_NB_CTL_L0	11
11 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	HT_CPU_NB_CTL_H1	11
11 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	HT_CPU_NB_CTL_L1	11

SKT-CPU638P-GP-U
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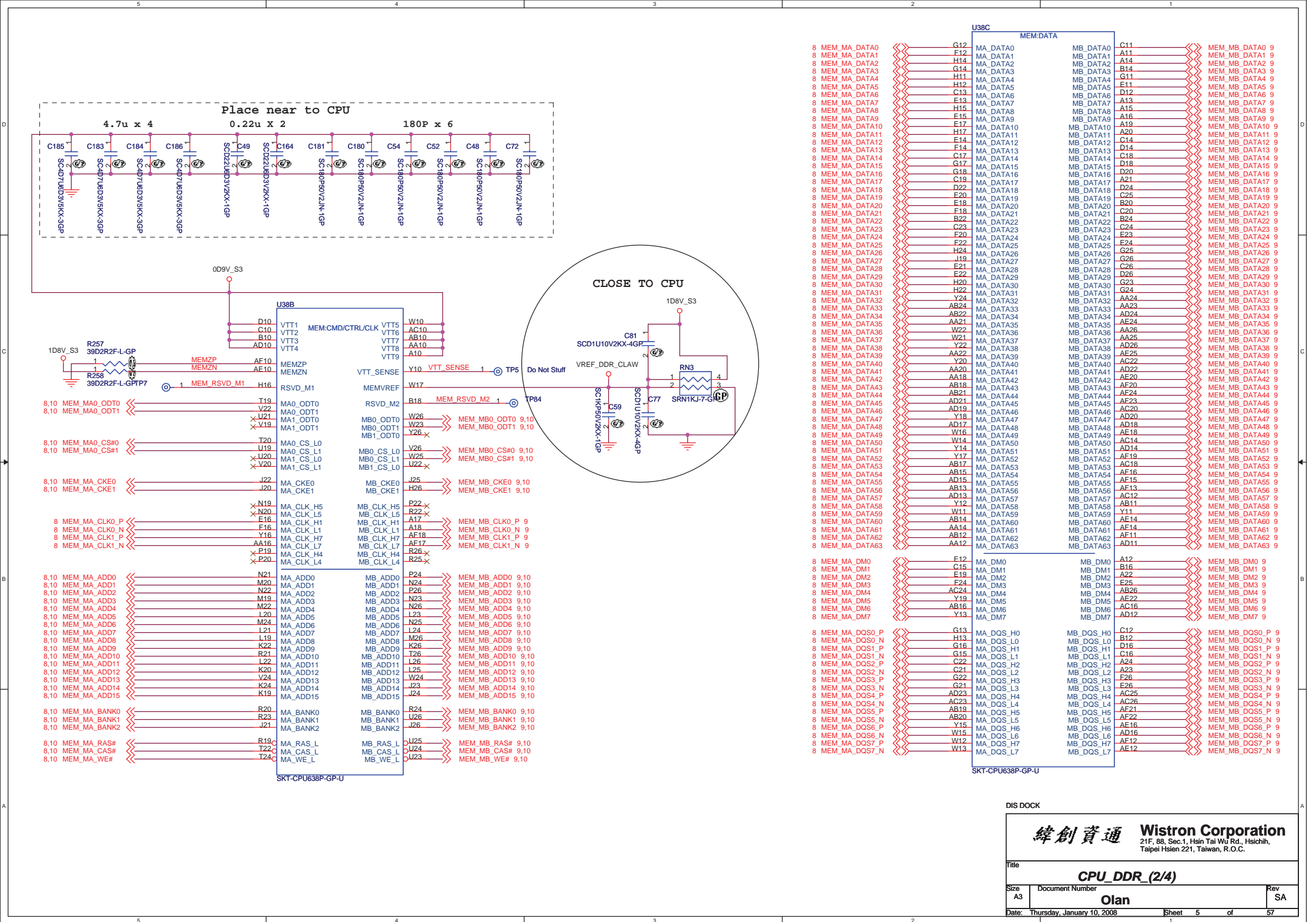
SKT-BGA638H176

State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
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	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

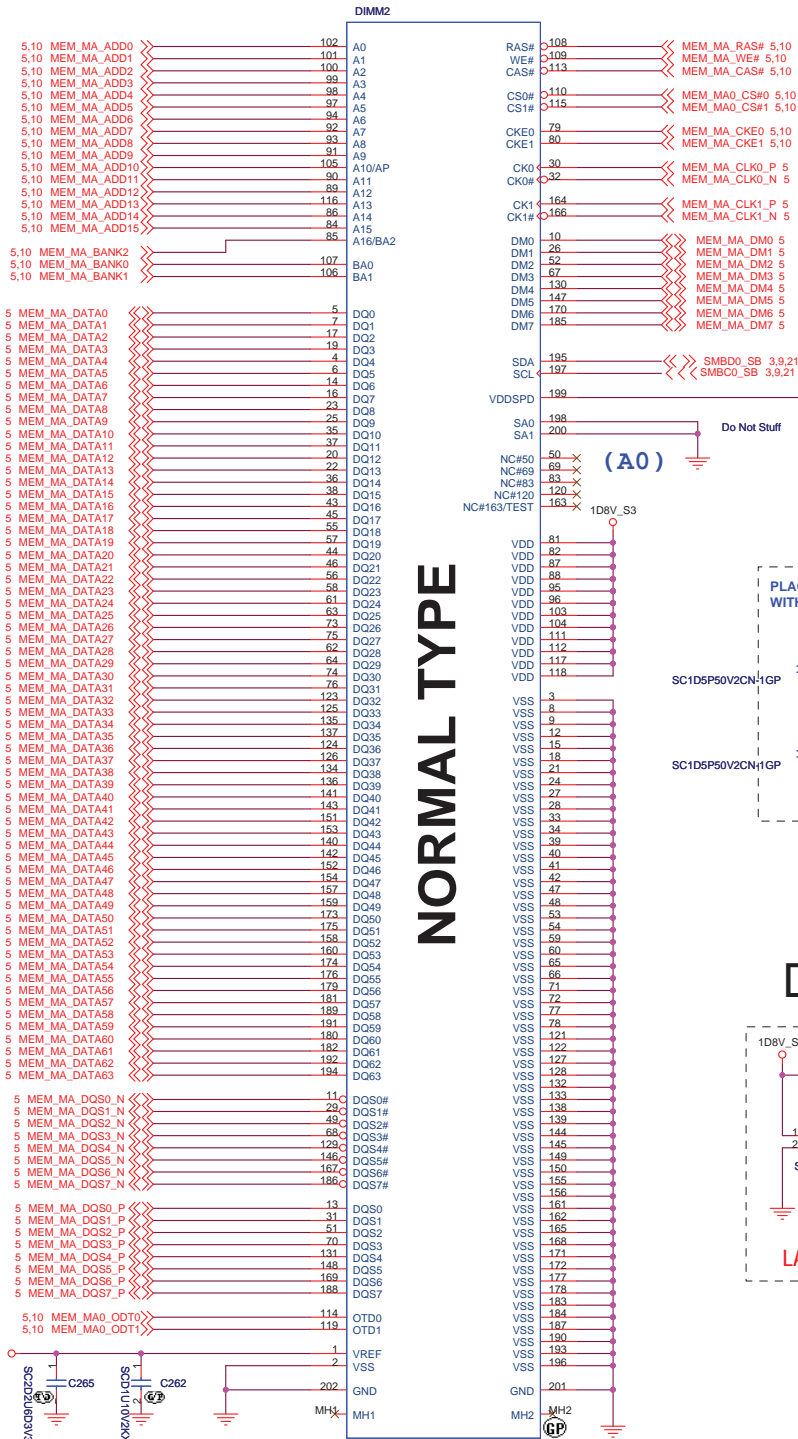
DIS DOCK

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Taipei Hsien 221, Taiwan, R.O.C.

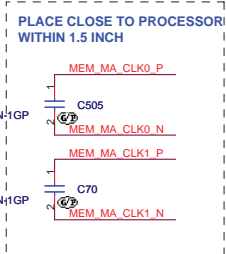
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Size	Document Number	Rev			SA
A3	Olan				
Date:	Thursday, January 10, 2008	Sheet	4	of	57



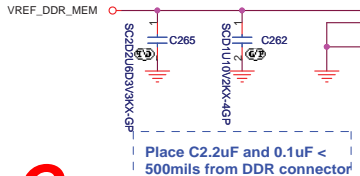
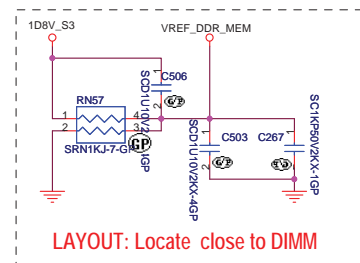




NORMAL TYPE



DDR_VREF

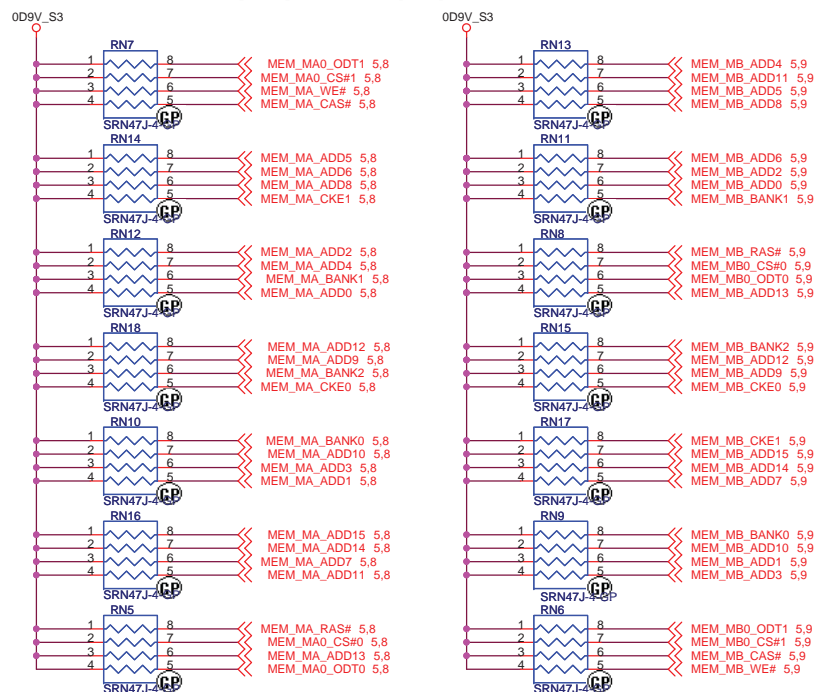


DDR2-200P-22-GP-U2
62.10017.A61
2ND = 62.10017.A51
HI 9.2mm

Main Source:

PARALLEL TERMINATION

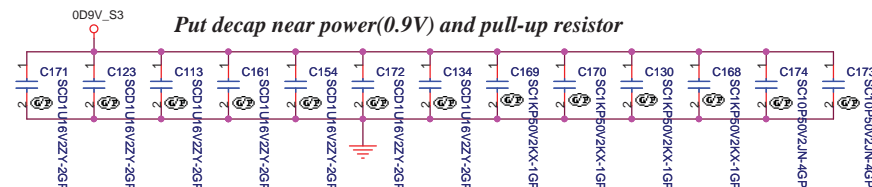
Put decap near power(0.9V) and pull-up resistor



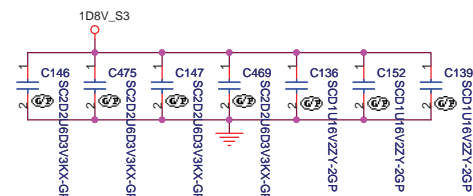
Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

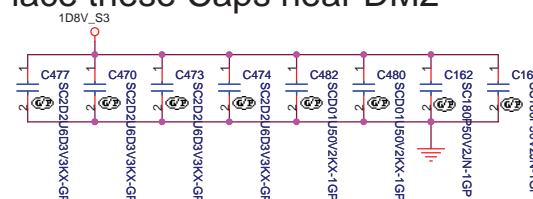


Place these Caps near DM1



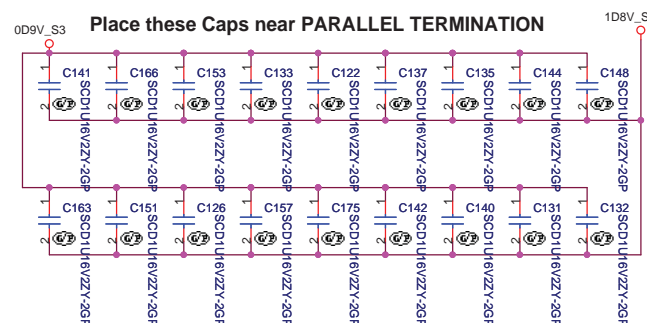
Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup
resistors terminated to 0D9V S3

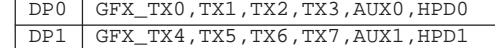
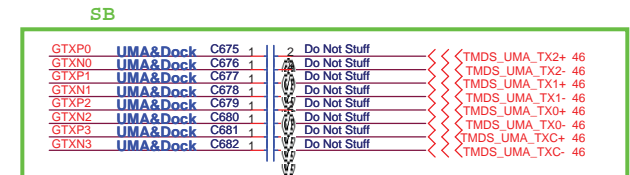
Place these Caps near PARALLEL TERMINATION

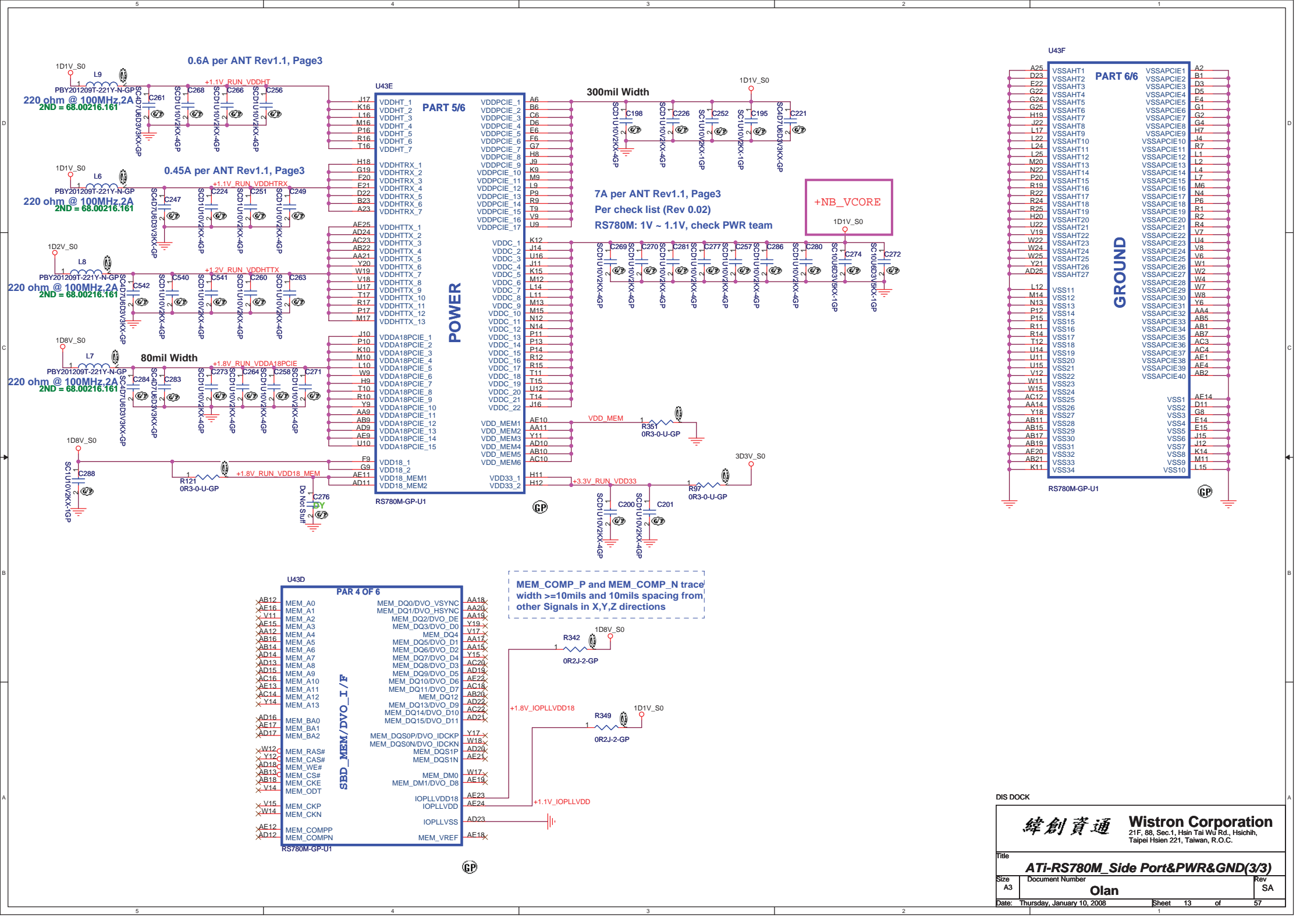


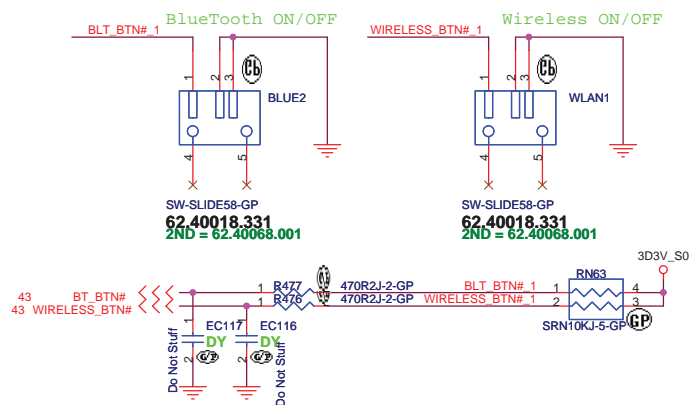
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Size A3	Document Number Olan	Rev SA
Date: Thursday, January 10, 2008	Sheet 10 of	57





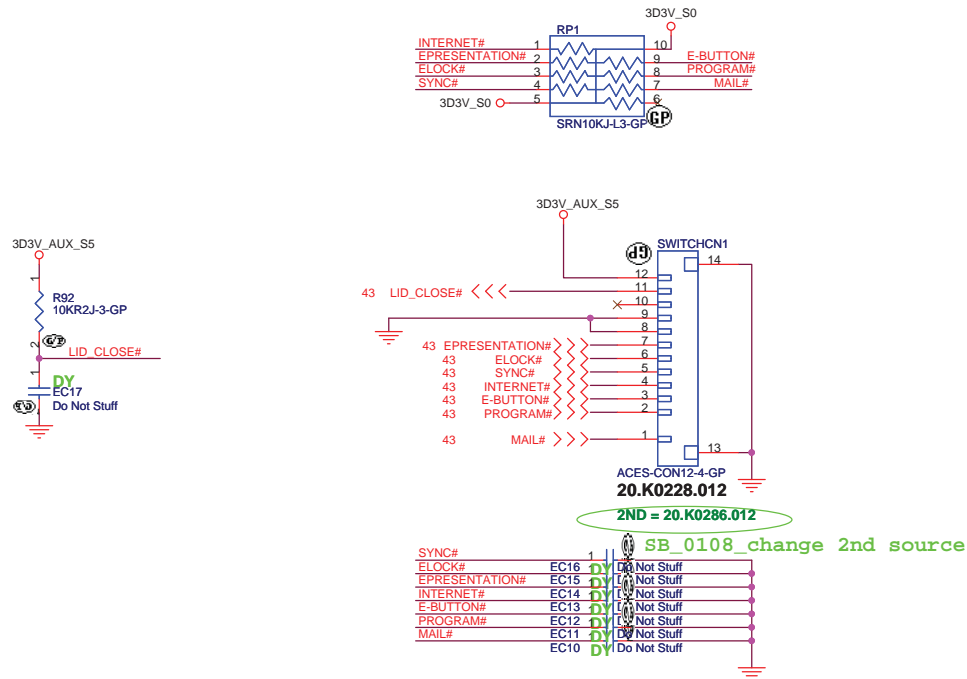


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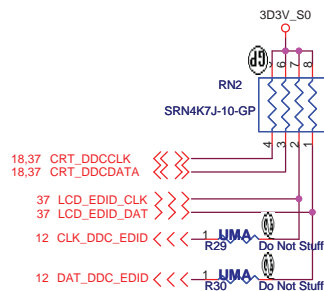
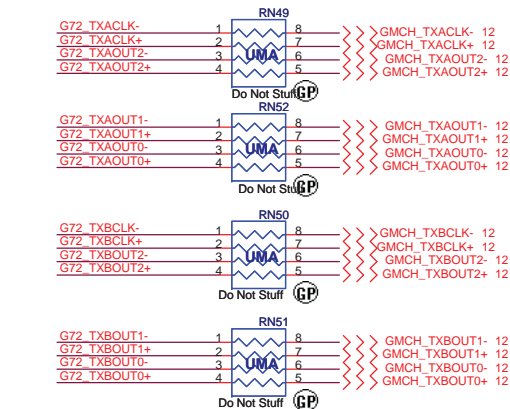
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Size	Document Number			Rev
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Date:	Thursday, January 10, 2008		Sheet 14 of	57

LAUNCH



DIS DOCK

WWW.AliSaler.Com



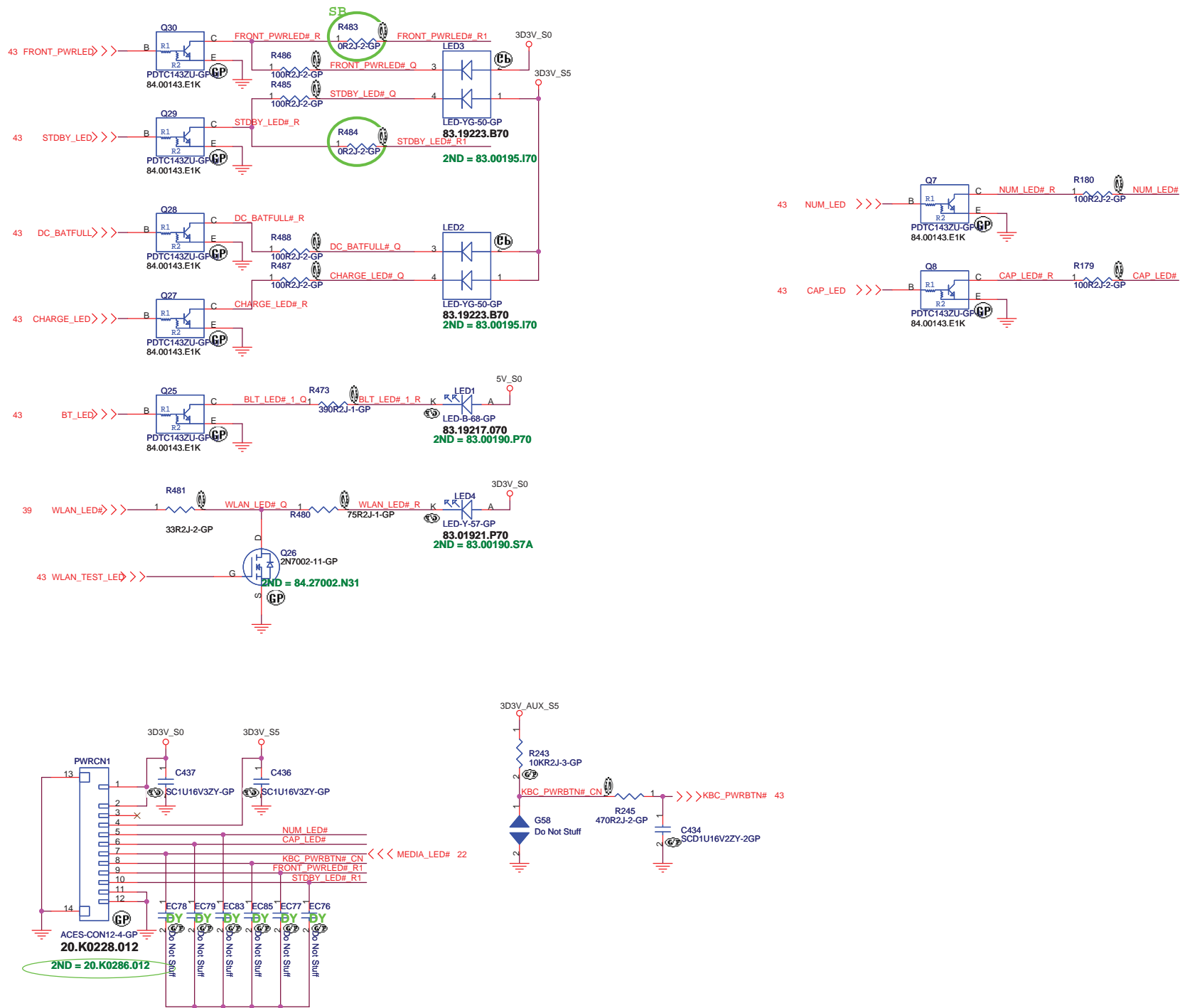
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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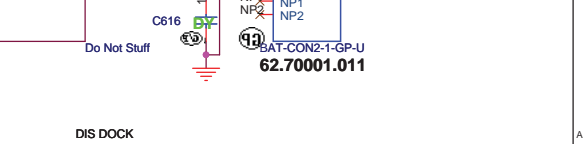
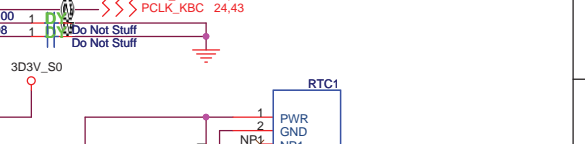
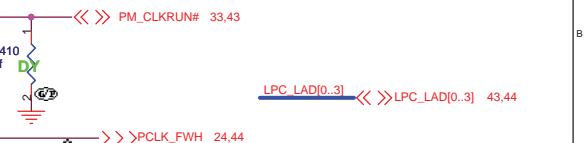
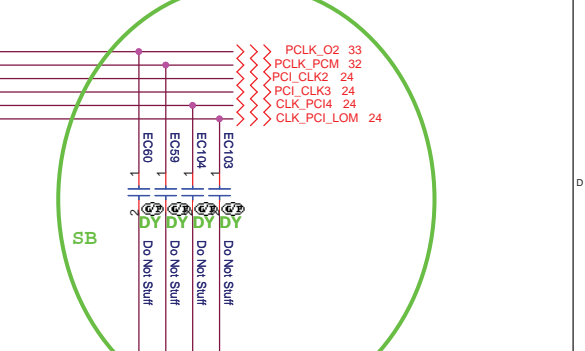
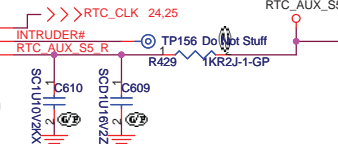
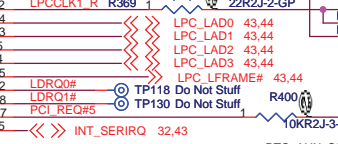
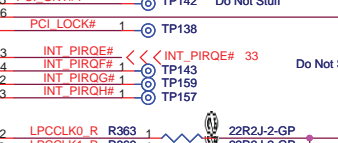
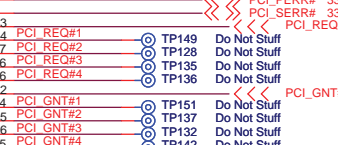
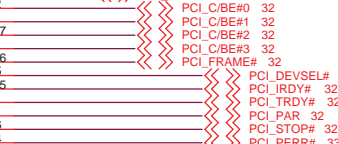
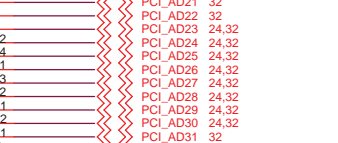
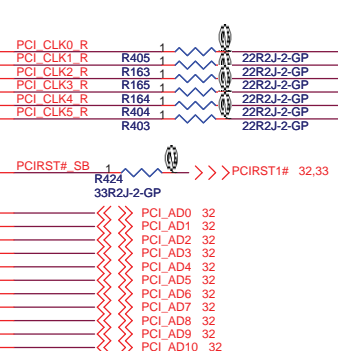
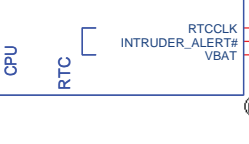
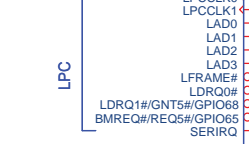
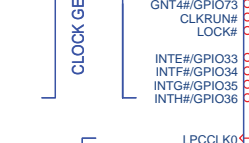
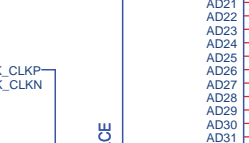
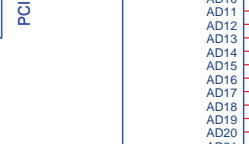
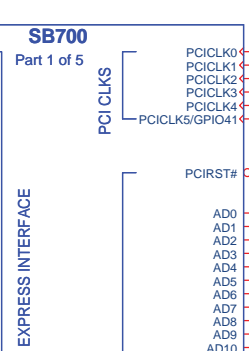
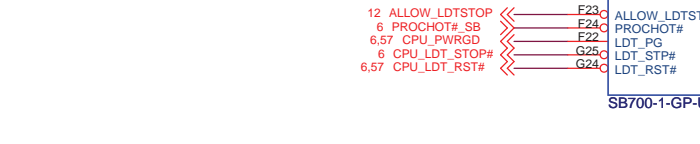
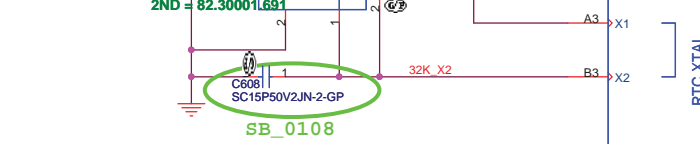
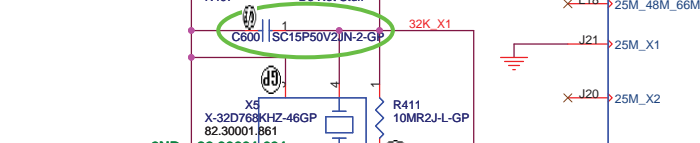
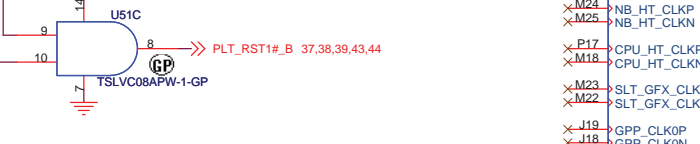
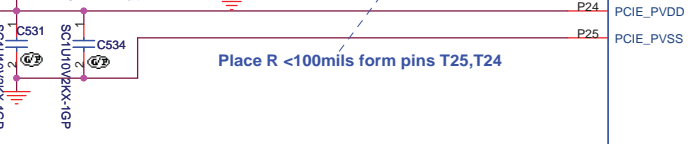
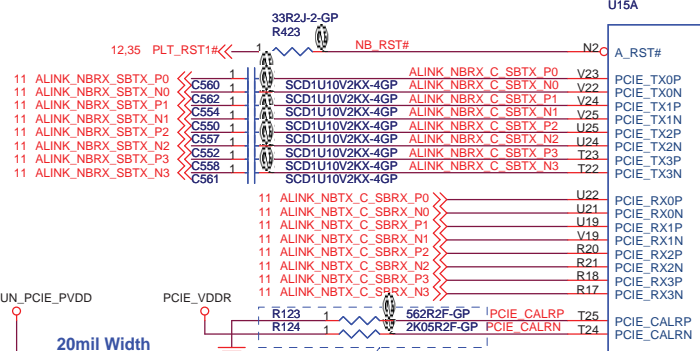
LCD CONN

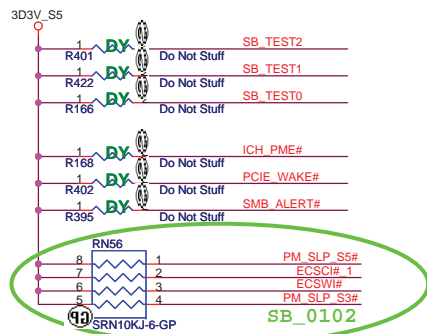
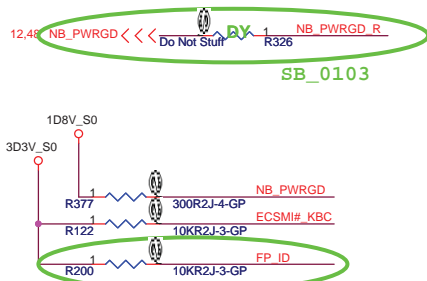
Olan

Rev	
SA	

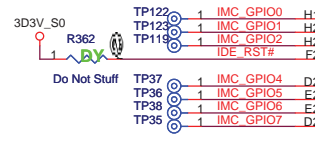
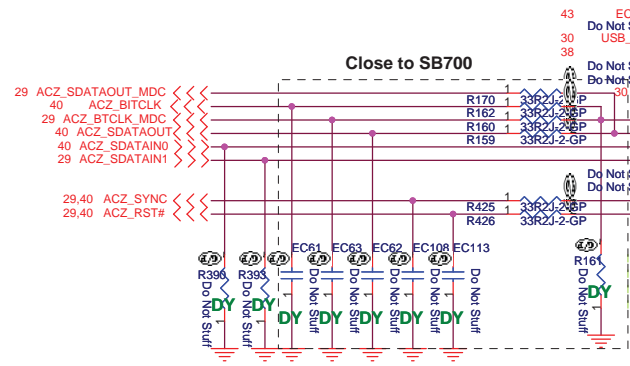
LED





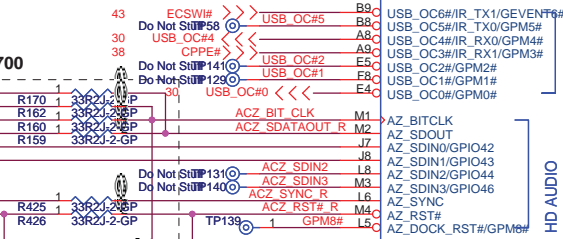


Close to SB700

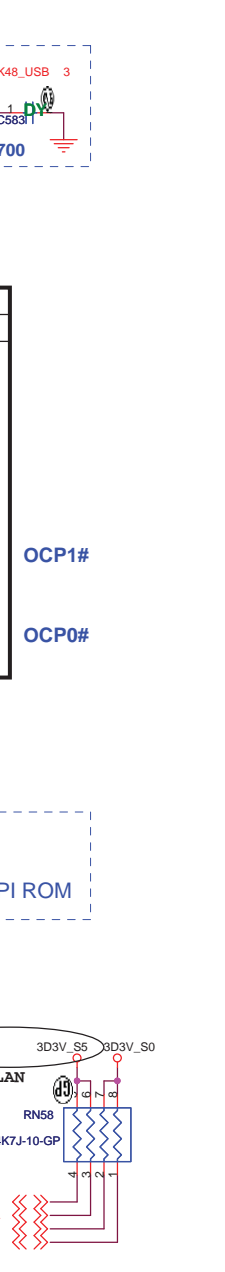
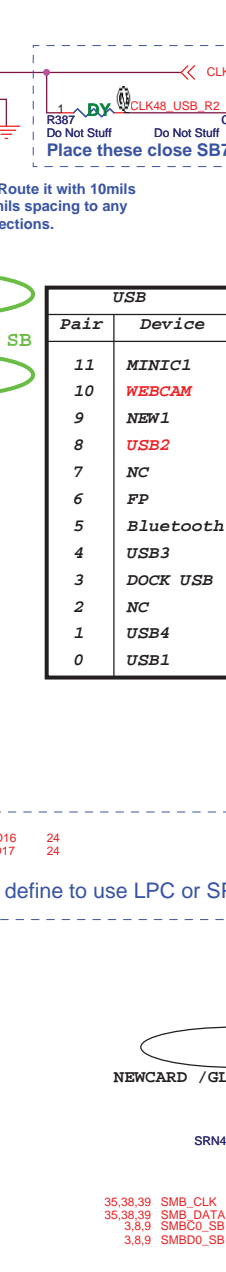
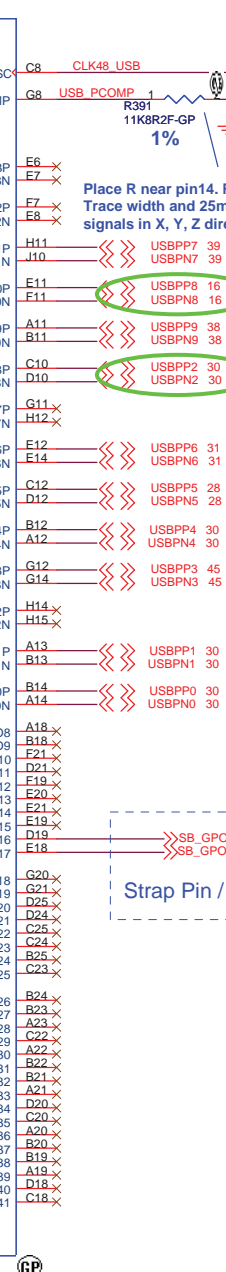
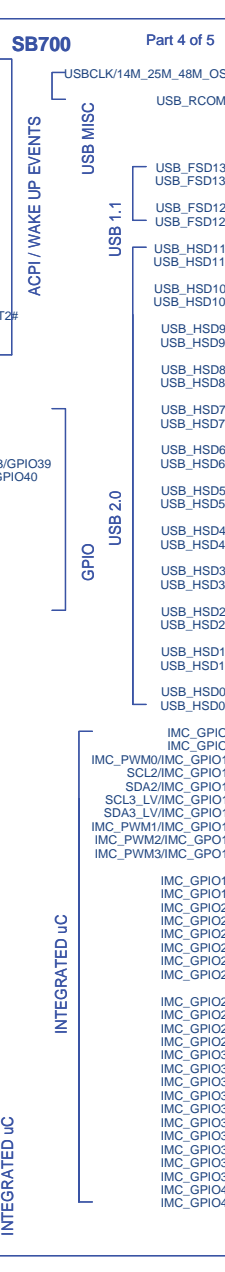
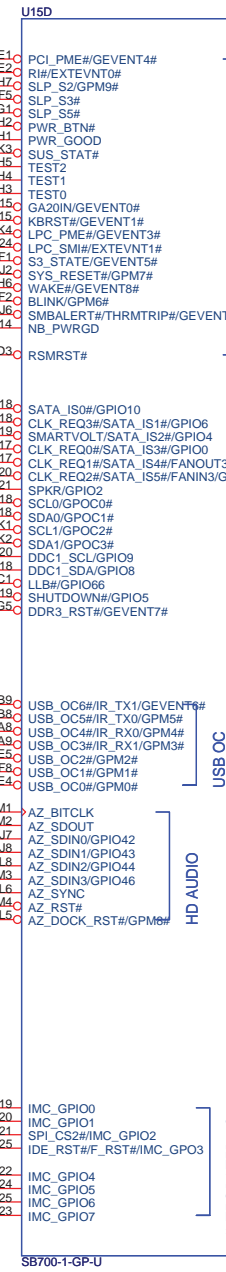


SB

18,40,43,45,46 DOCK_DT1# >>> Do Not Stuff R320



TO STRAPS



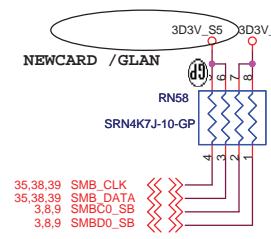
Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

USB	
Pair	Device
11	MINIC1
10	WEBCAM
9	NEW1
8	USB2
7	NC
6	FP
5	Bluetooth
4	USB3
3	DOCK USB
2	NC
1	USB4
0	USB1

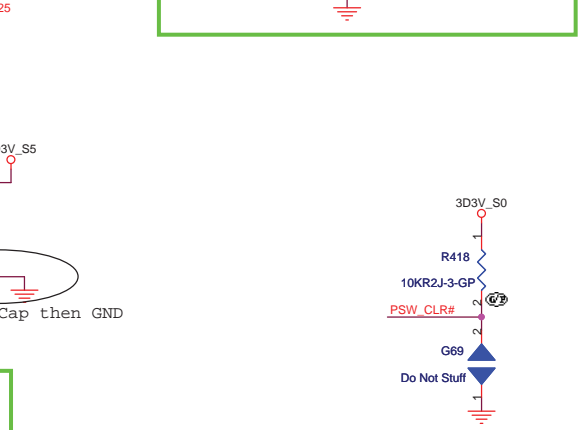
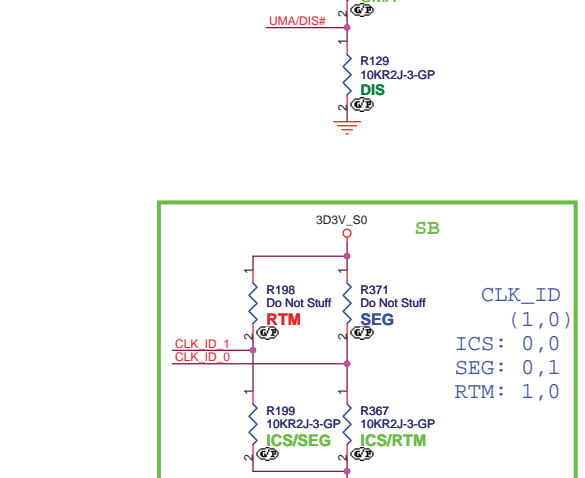
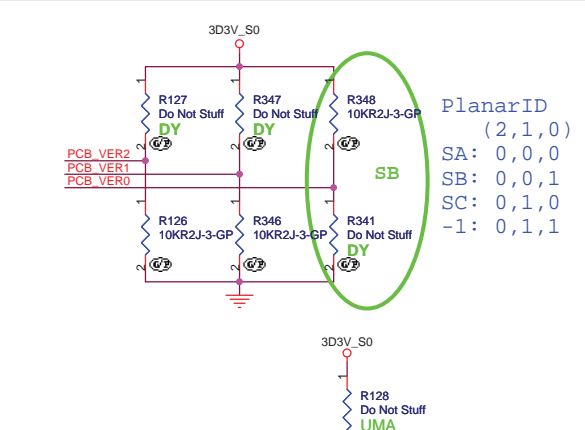
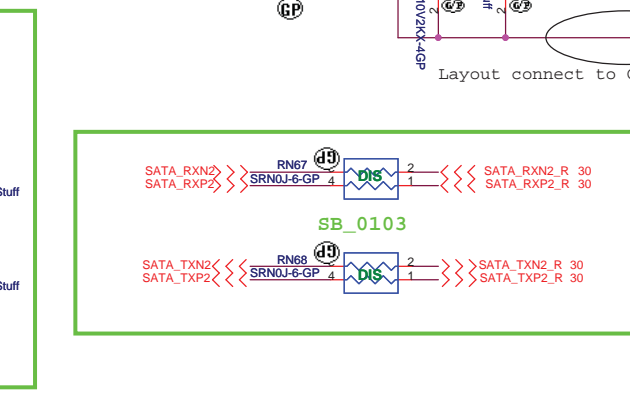
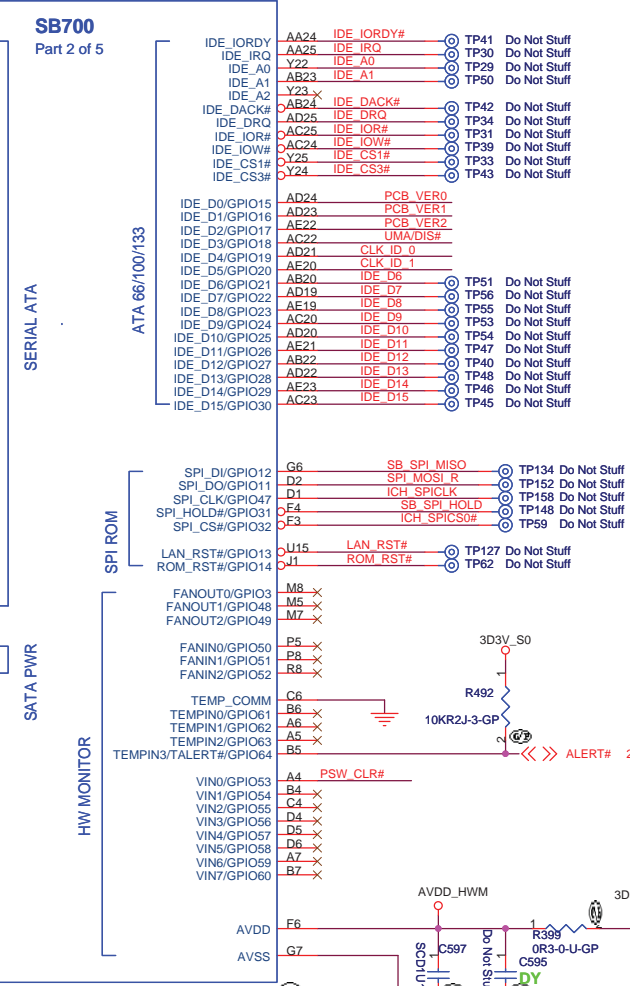
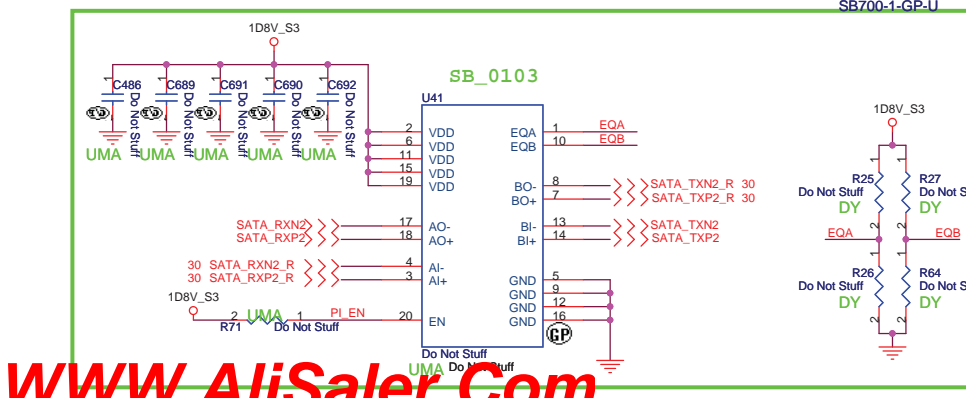
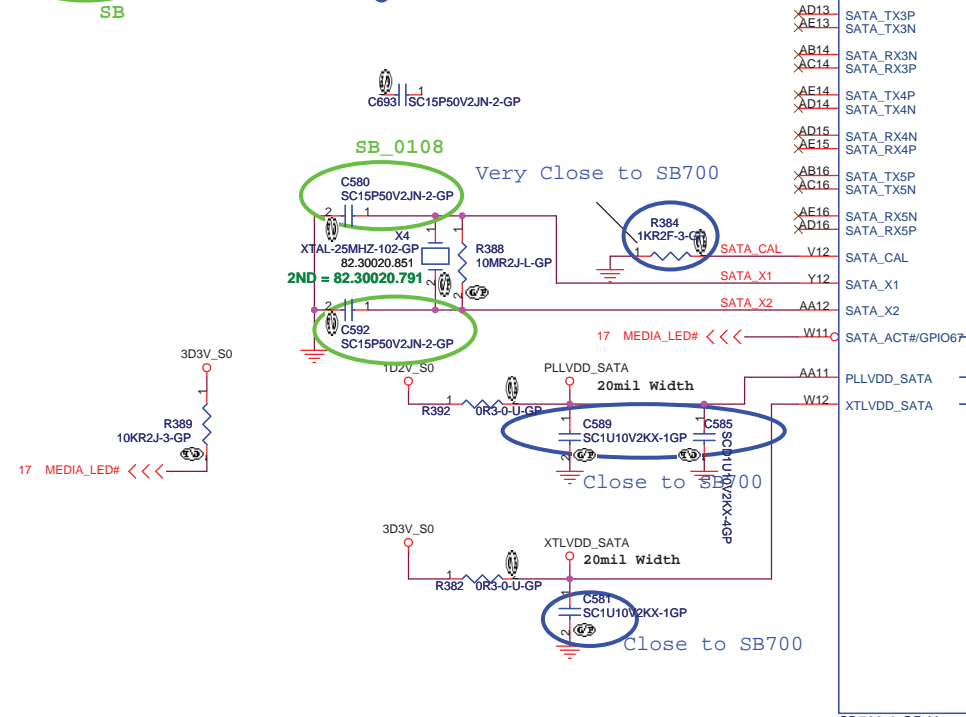
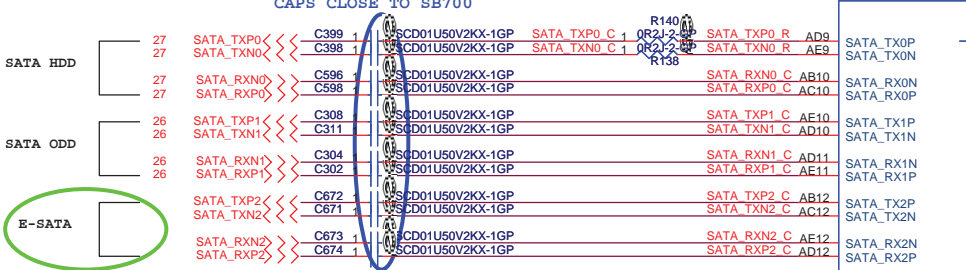
OCP1#

OCP0#

Strap Pin / define to use LPC or SPI ROM



PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700



DIS DOCK

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ATI-SB700 SATA-IDE (3/5)

Size A3 Document Number

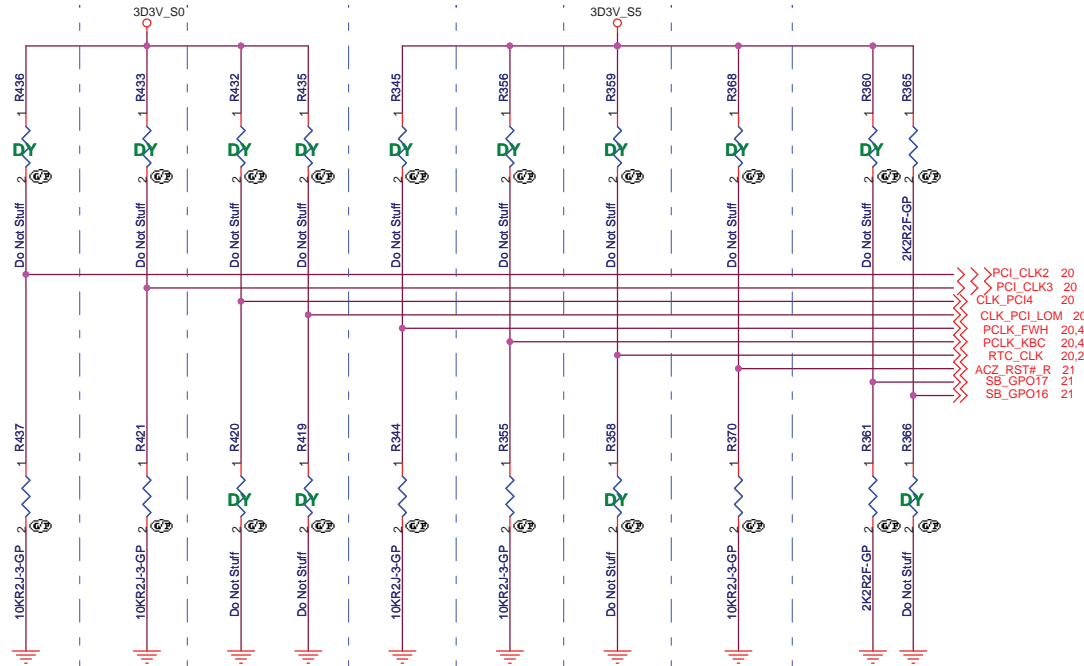
Date: Thursday, January 10, 2008

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Rev SA

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



PCI_CLK2 20
 PCI_CLK3 20
 CLK_PCI4 20
 CLK_PCI_LOM 20
 PCLK_FWH 20,44
 PCLK_KBC 20,43
 RTC_CLK 20,25
 ACZ_RST#_R 21
 SB_GPO17 21
 SB_GPO16 21

DEBUG STRAPS

Do Not Stuff 160 PCI_AD23 20,32
 Do Not Stuff 163 PCI_AD24 20,32
 Do Not Stuff 161 PCI_AD25 20,32
 Do Not Stuff 162 PCI_AD26 20,32
 Do Not Stuff 164 PCI_AD27 20,32
 Do Not Stuff 165 PCI_AD28 20,32
 Do Not Stuff 166 PCI_AD29 20,32
 Do Not Stuff 153 PCI_AD30 20,32

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

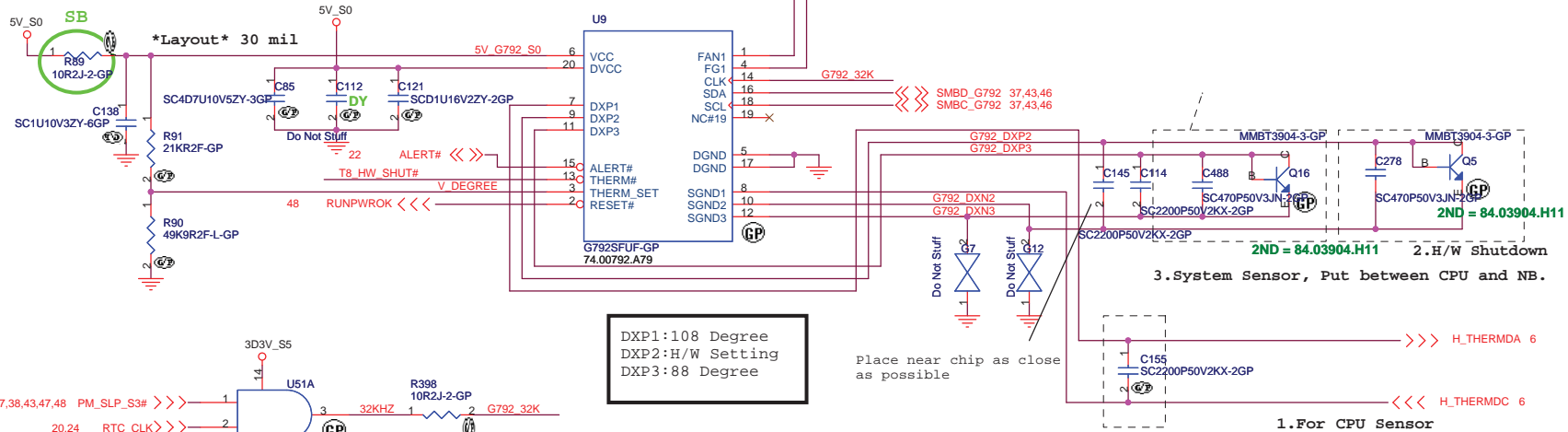
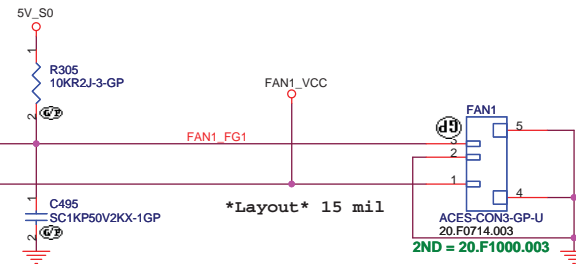
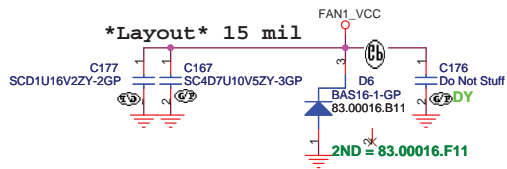
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

DIS DOCK

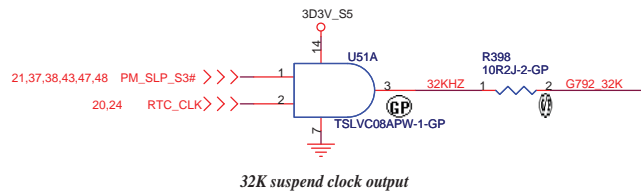
緯創資通 Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		ATI-SB700 STRAPPING (5/5)	
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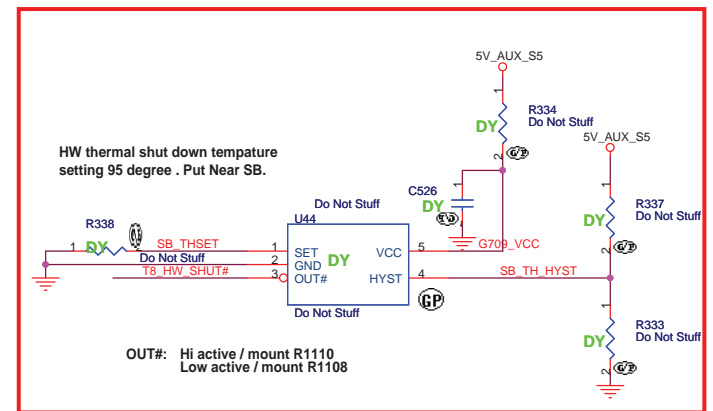
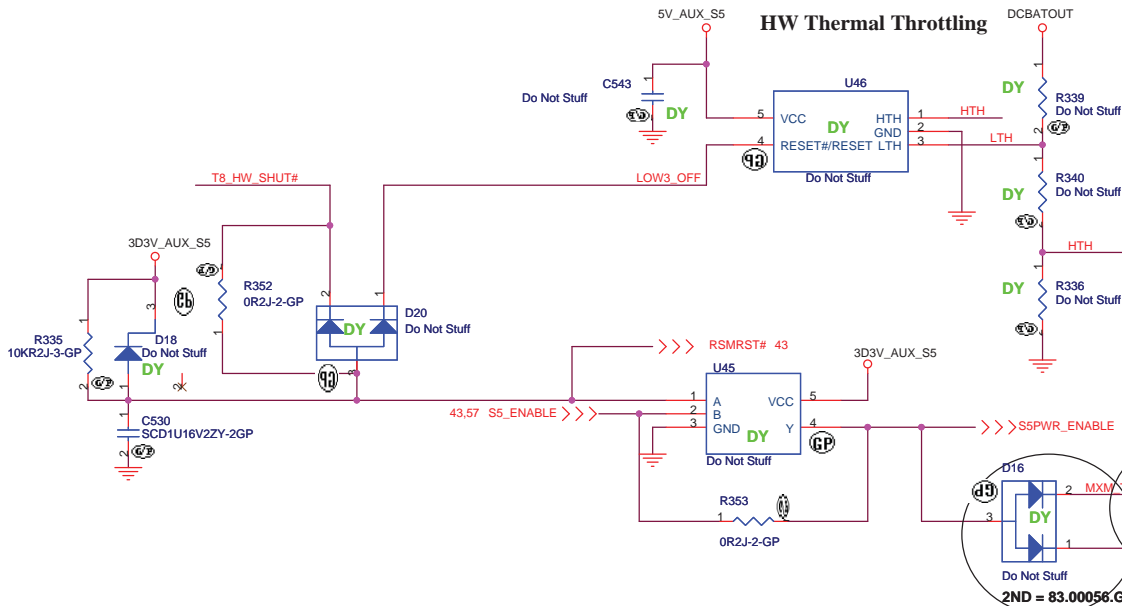
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree

Place near chip as close as possible



BL3#

HW Thermal Throttling

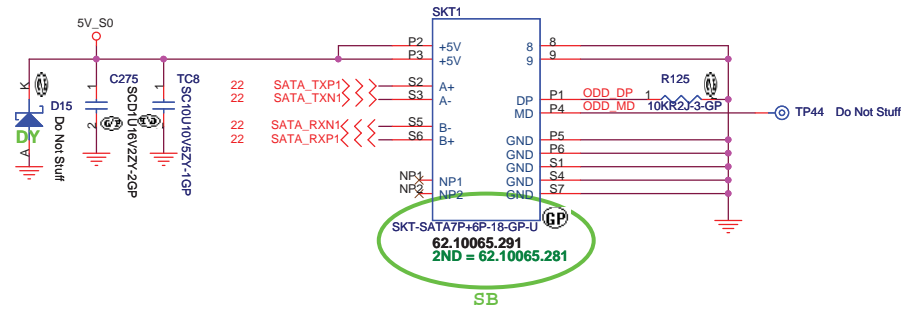


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Title			G792	
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ODD Connector

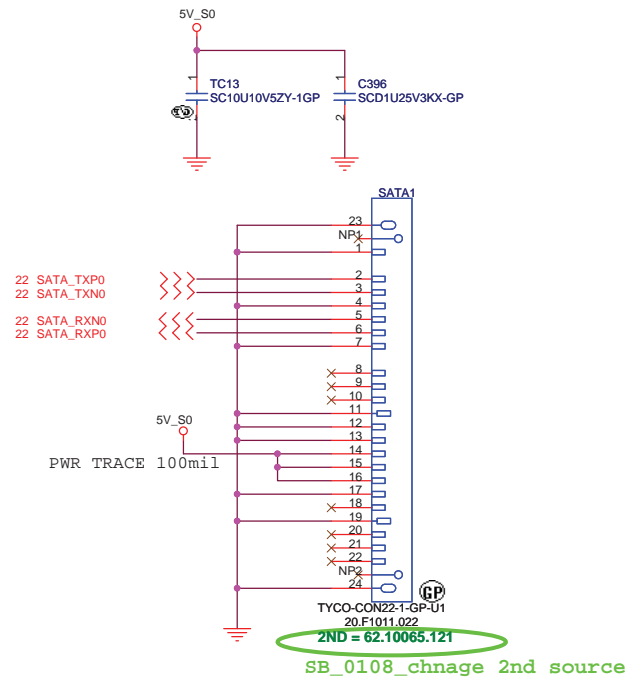


DIS DOCK

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Taipei Hsien 221, Taiwan, R.O.C.

Title				
CDROM				
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	Olan			SA
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SATA HDD Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD

Size

Document Number

Olan

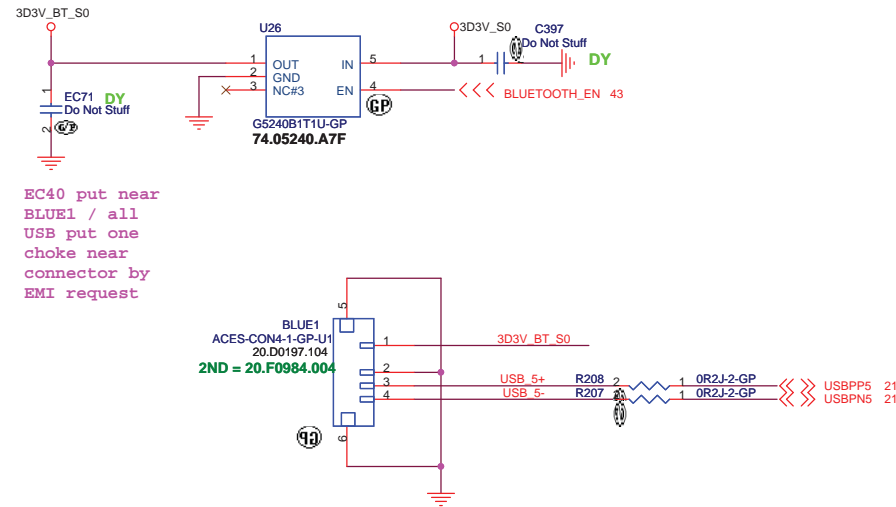
Rev

SA

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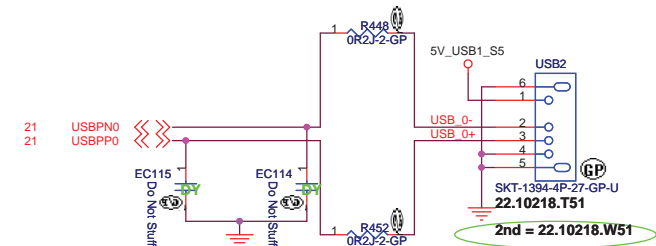
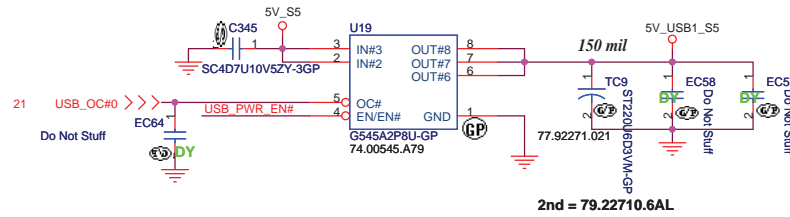
BLUETOOTH MODULE



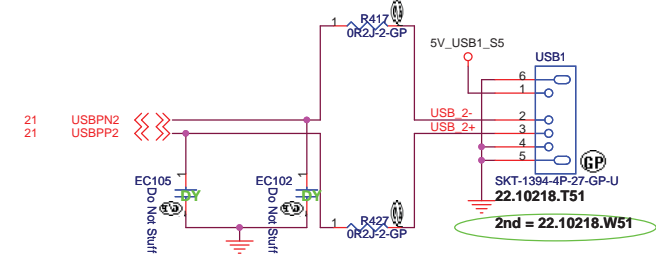
DIS DOCK

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

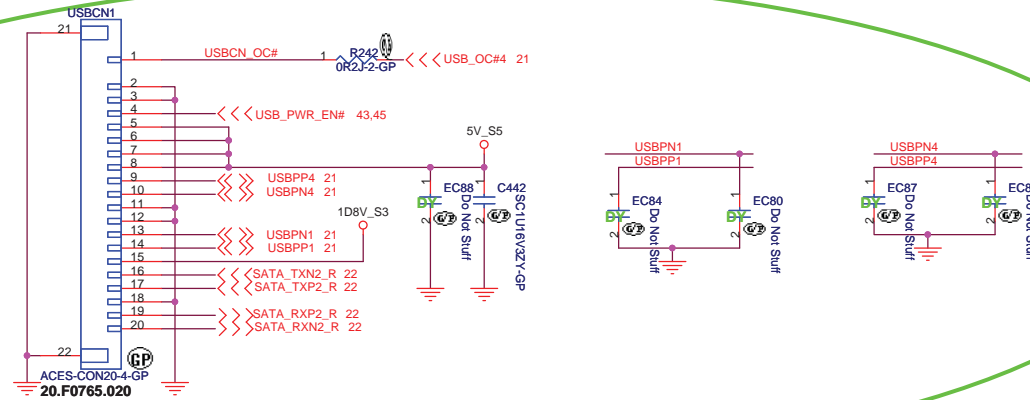
Title				
BLUETOOTH				
Size	Document Number			Rev
	Olan			SA
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SB_0108_change 2nd source



SB_0102

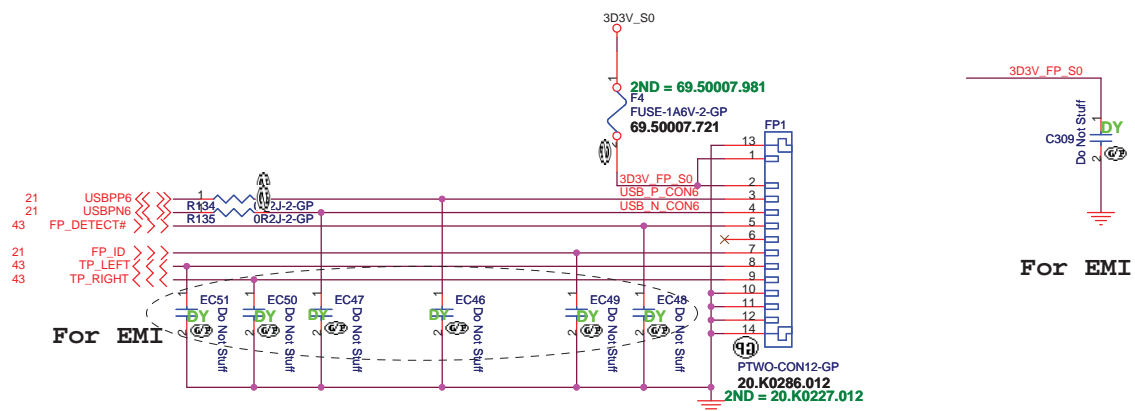


DIS DOCK

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Title				
USB				
Size	Document Number			Rev
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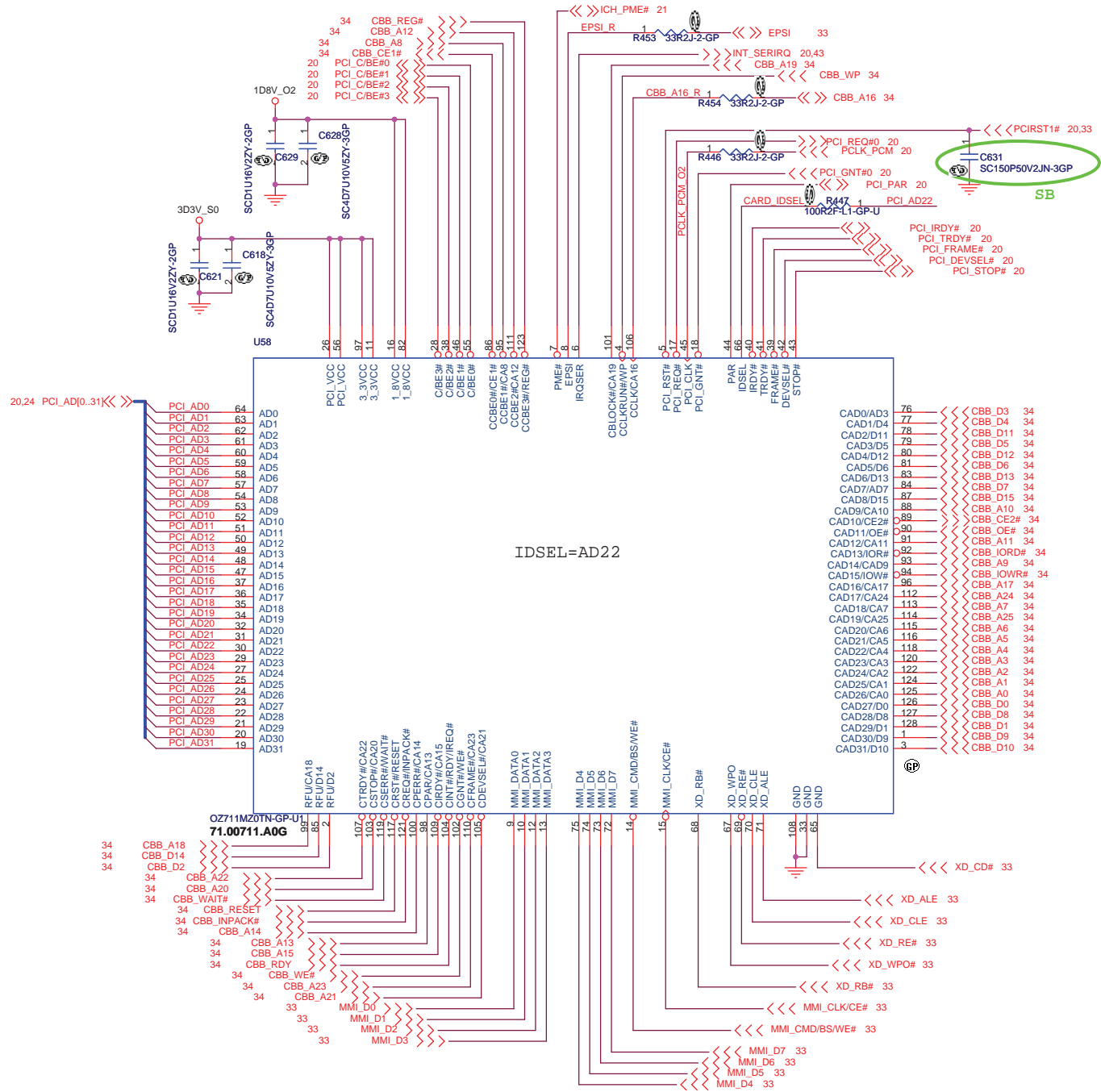
Finger printer

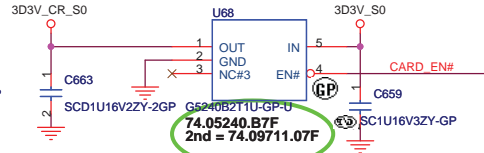
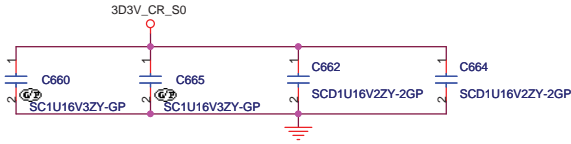


DIS DOCK

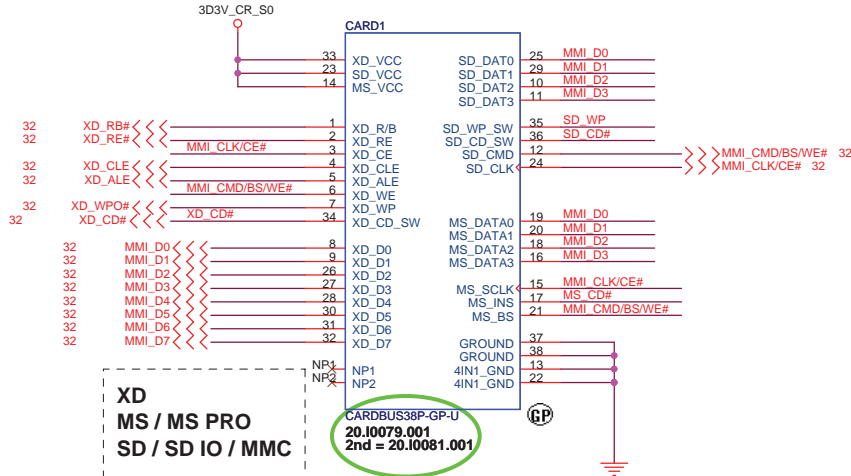
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Title		
Finger Printer		
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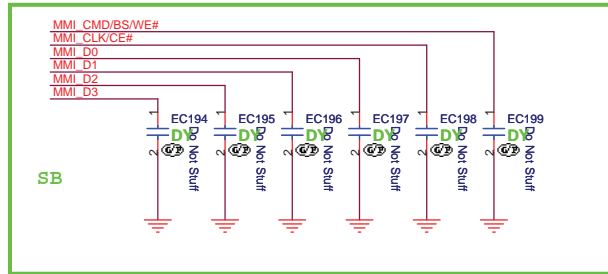
ENG Add 2nd source



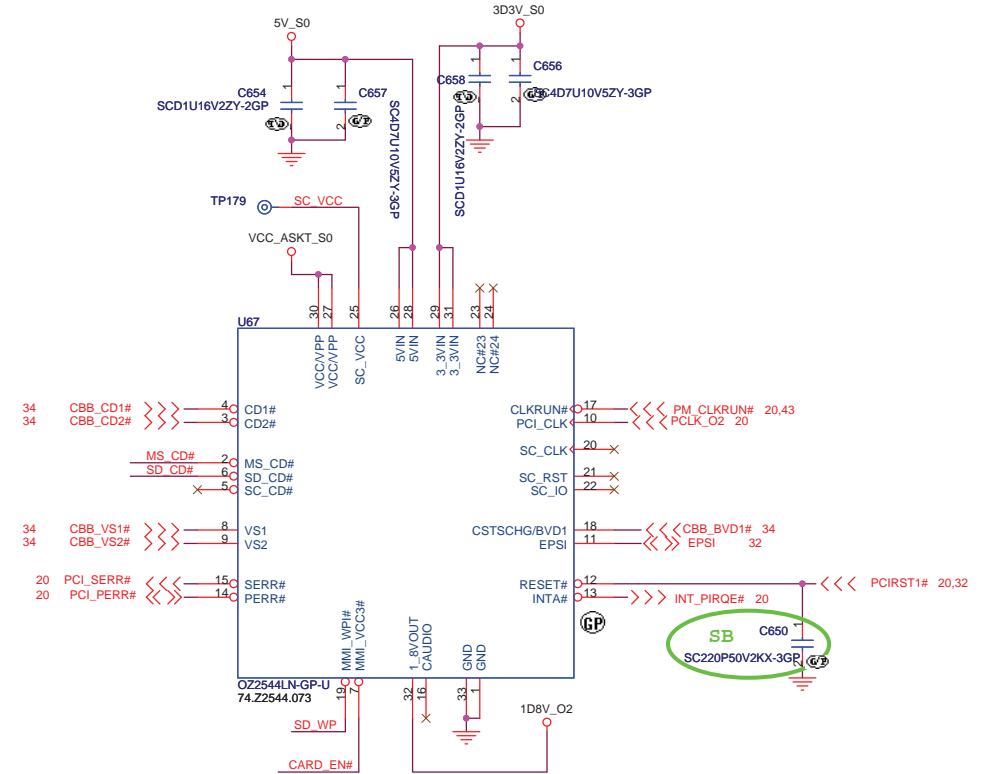
XD
MS / MS PRO
SD / SD IO / MMC

CARDBUS38P-GP-U
20.10079.001
2nd = 20.10081.001

SB



SB



SB
C650
SC220P50V2KX-3GR

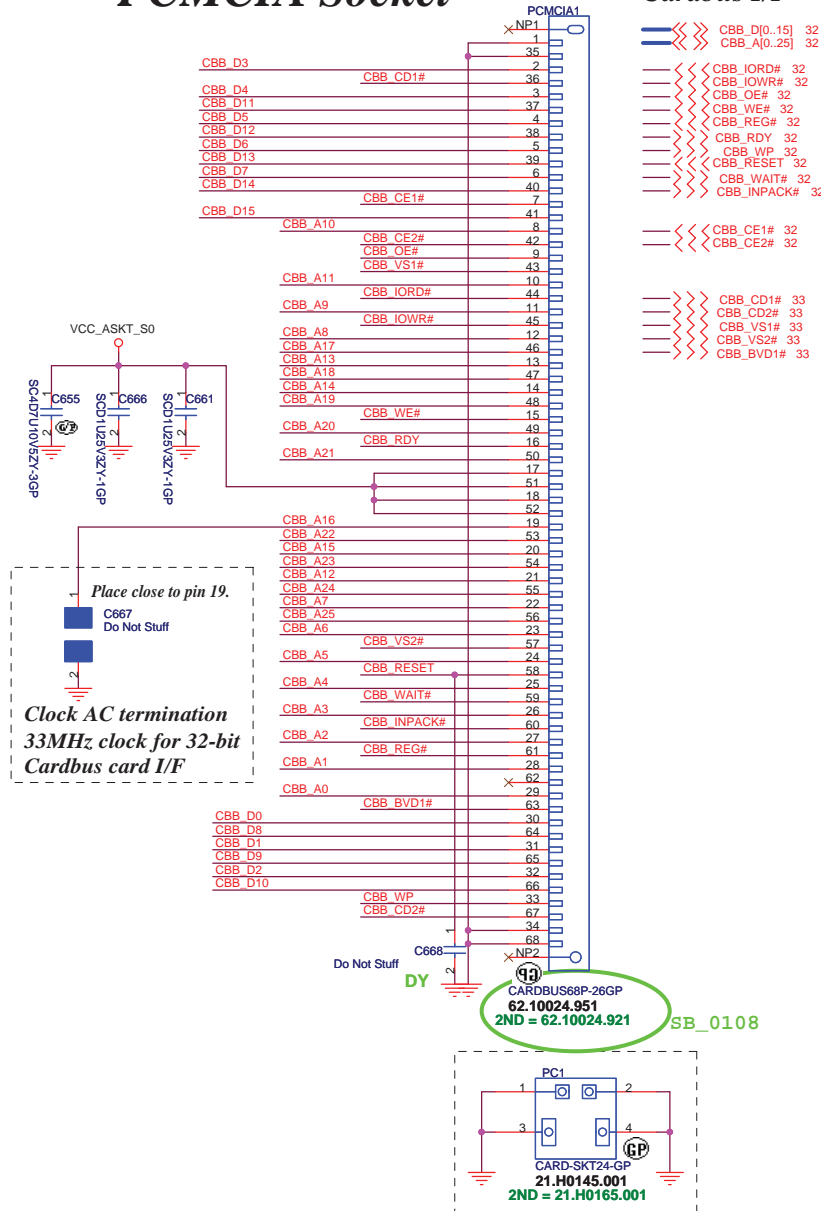
DIS DOCK

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Title
Size A3 Document Number
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Card Reader Connector
Olan
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PCMCIA Socket

Cardbus I/F



DIS DOCK

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Taipei Hsien 221, Taiwan, R.O.C.

Title

PCMCIA

Size
A3

Document Number

Olan

Rev
SA

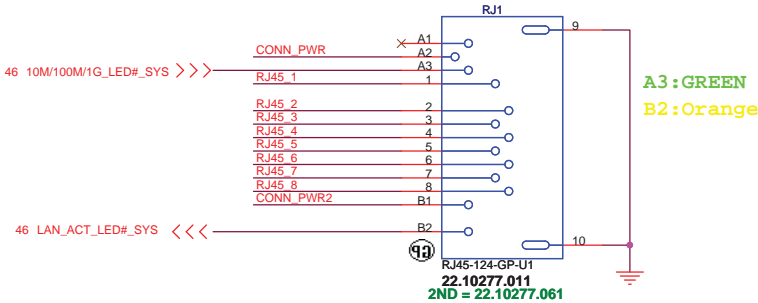
Date: Thursday, January 10, 2008

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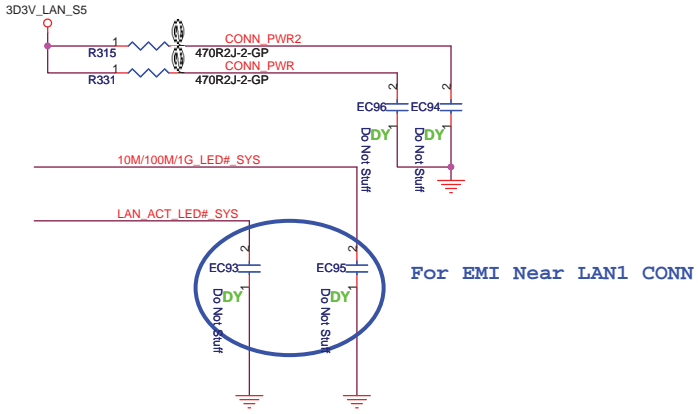
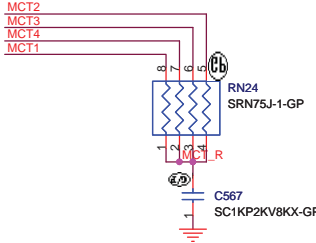
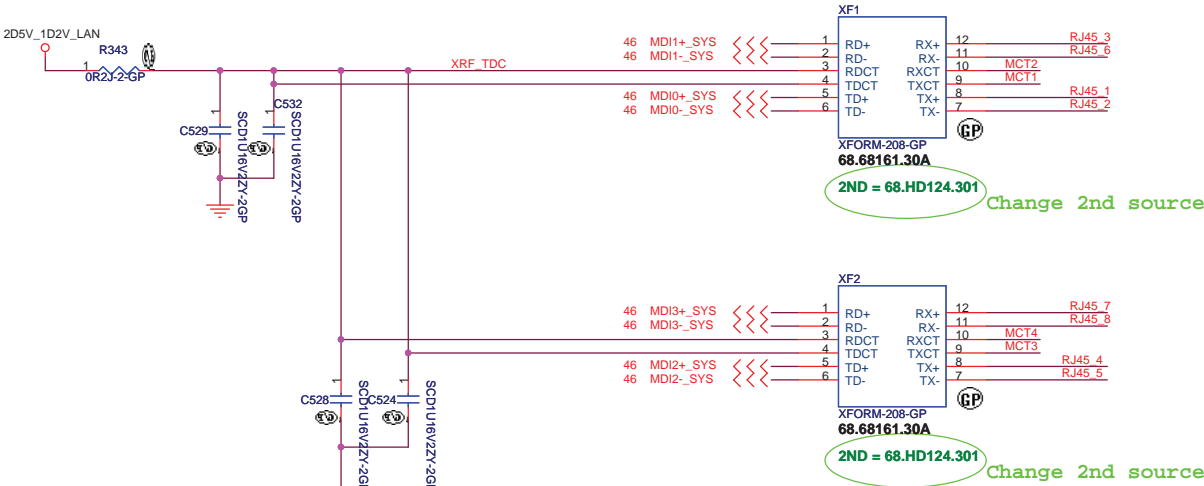
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

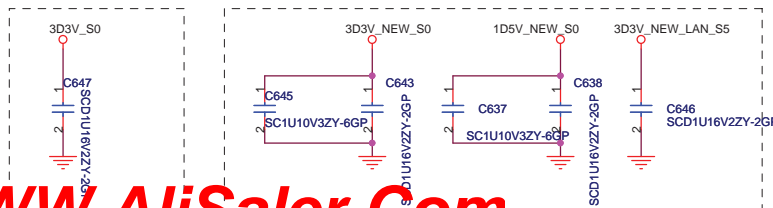
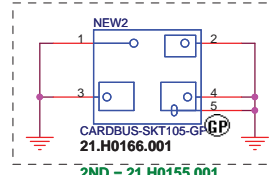


LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

GIGA Lan Transformer

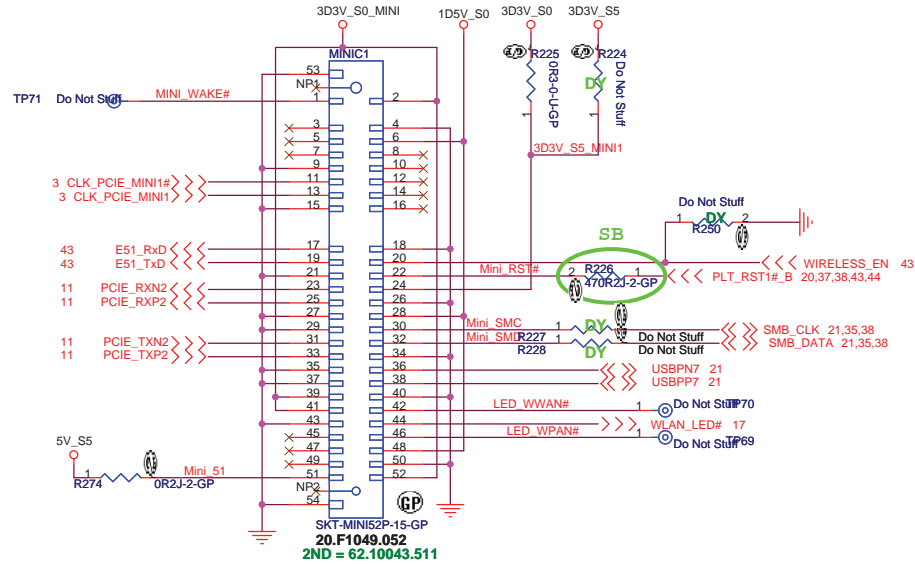


26
1

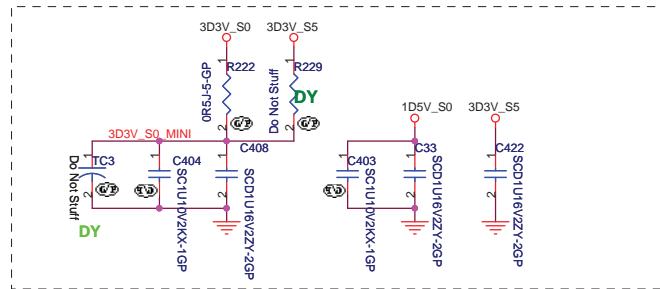


Title			
NEW CARD			
Size	Document Number		Rev
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Mini Card Connector(WLAN)



Place near MINIC1



DIS DOCK

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	Title
--	-------

Mini Card

Size	Document Number
------	-----------------

A3

Olan

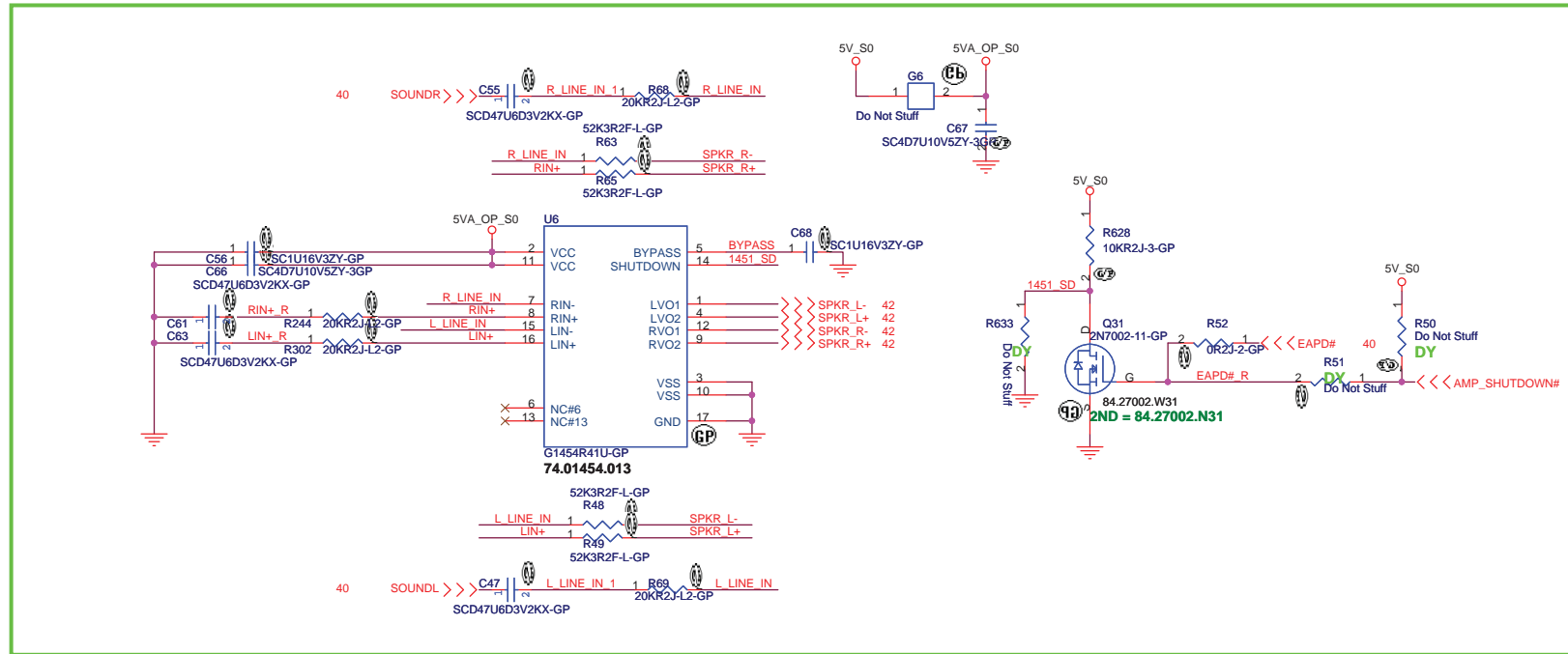
Rev
SA

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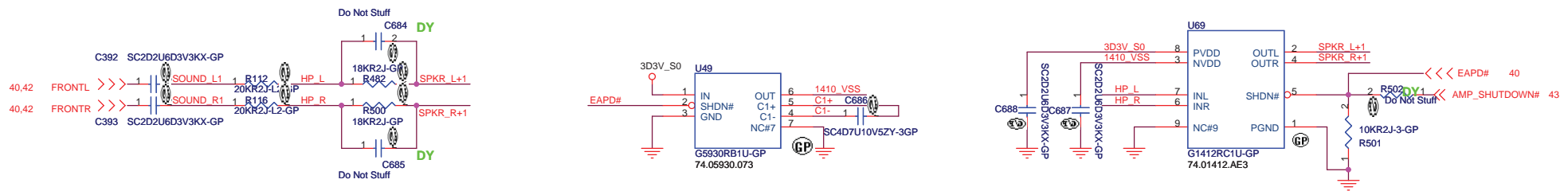
AUDIO OP AMPLIFIER

SB



SB

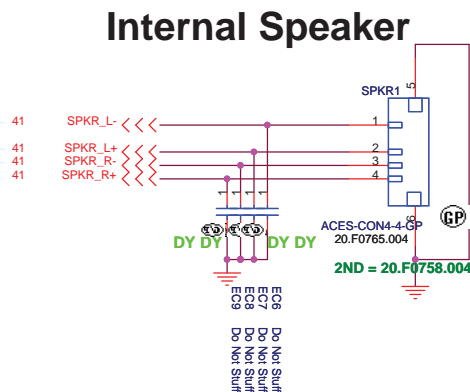
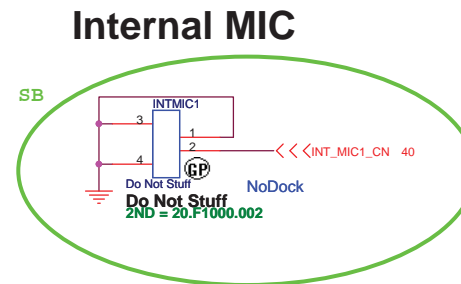
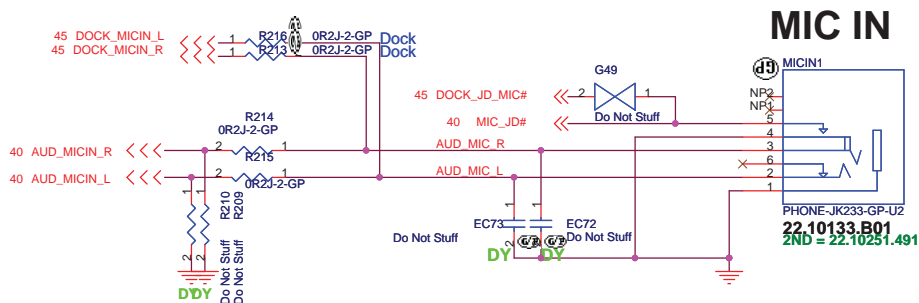
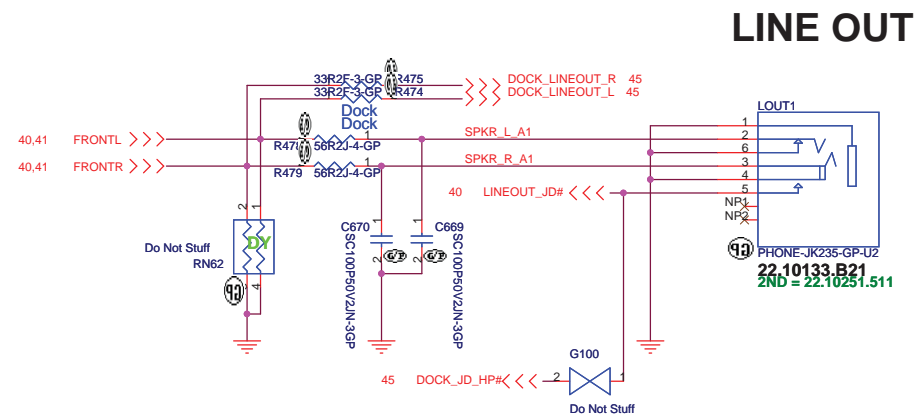
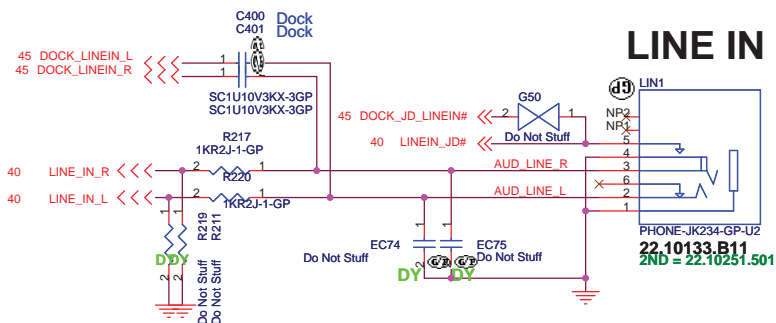
KBC_MUTE_GPIO8



DIS DOCK

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Title		
AUDIO AMP		
Size	Document Number	Rev
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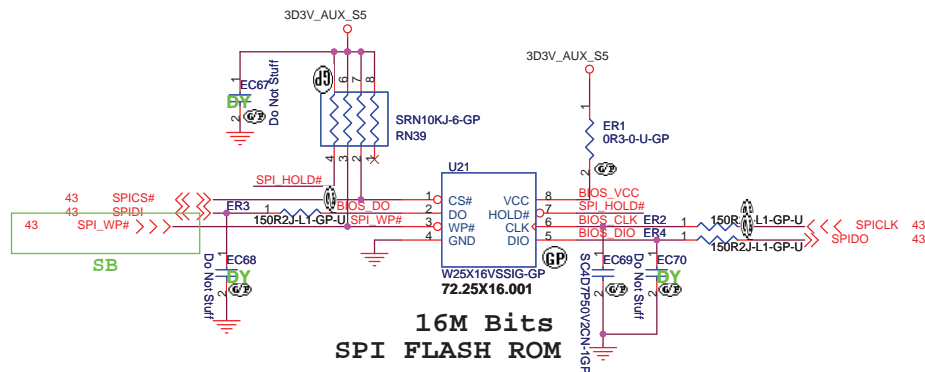


DIS DOCK

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Title			AUDIO JACK
Size	Document Number	Olan	
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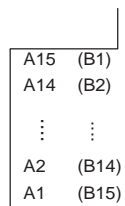
Rev
SB



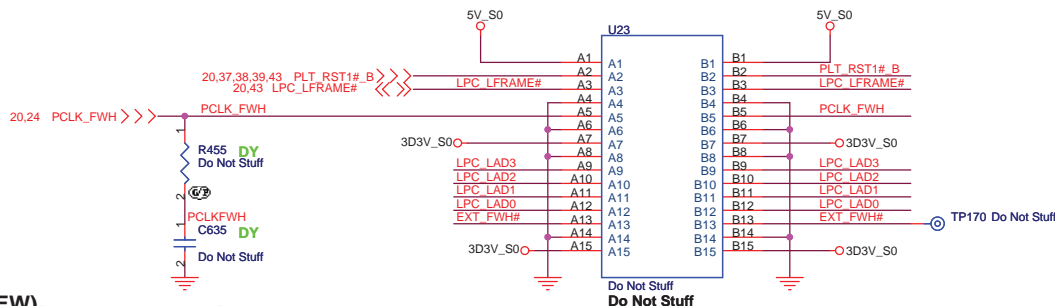
20,43 LPC_LAD[0..3] <<>> LPC_LAD[0..3]

GOLDEN FINGER FOR DEBUG BOARD

TOP VIEW



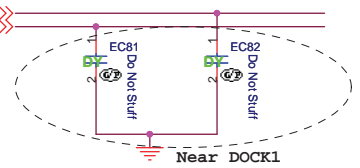
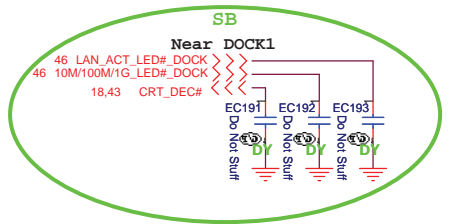
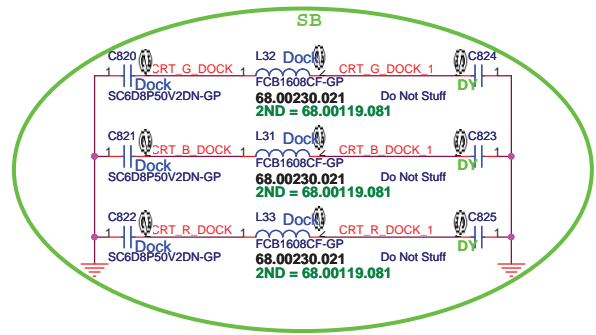
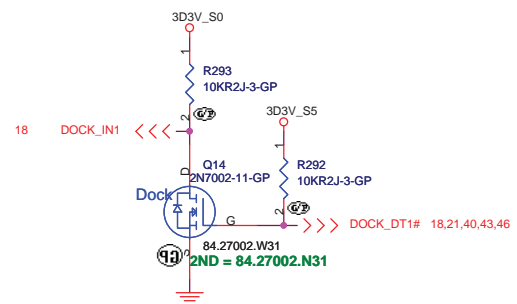
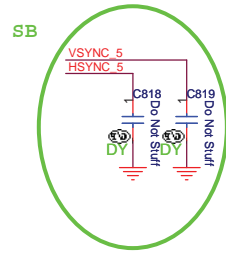
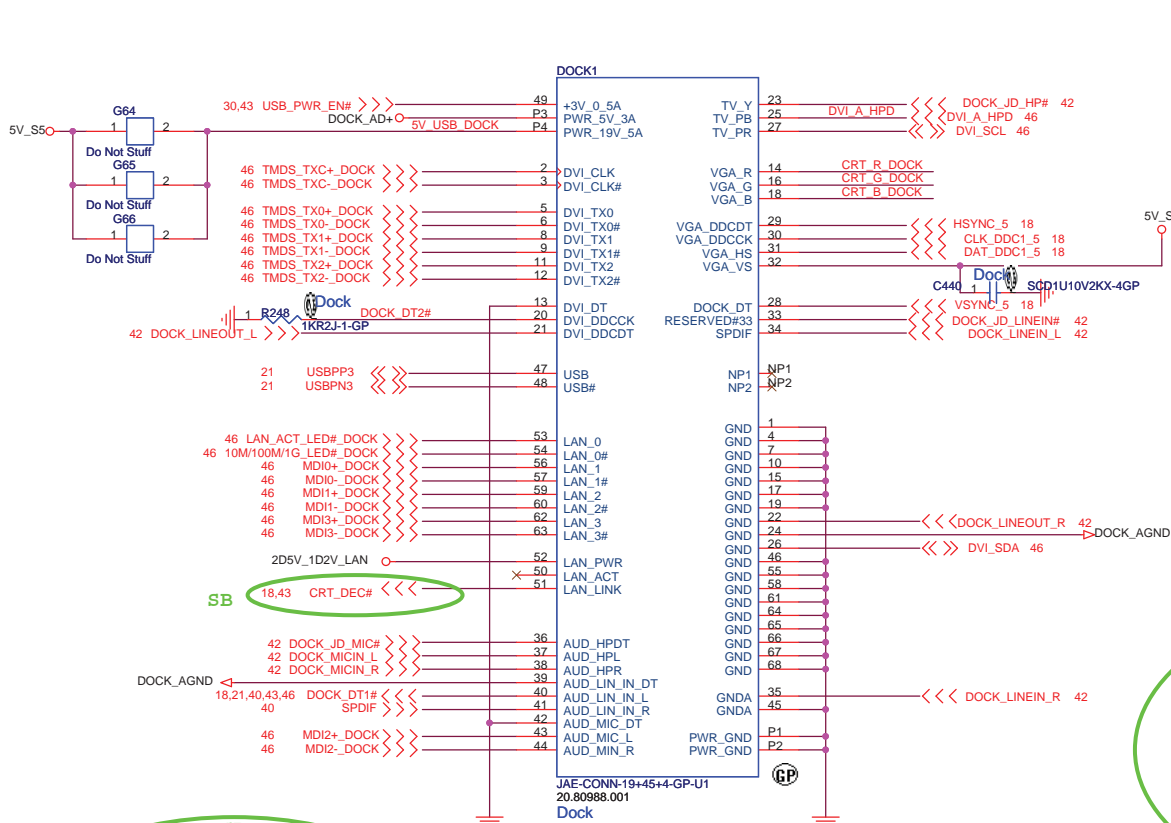
(BOTTOM VIEW)



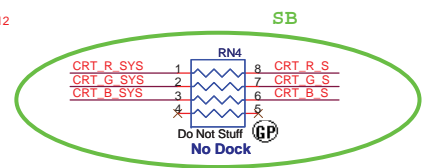
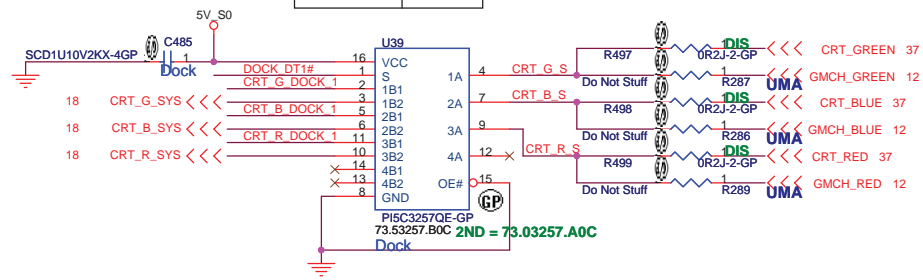
DIS DOCK

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Title			BIOS		
Size	Document Number				Rev
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Function	CRT
SYSTEM	H
DOCK	L



DIS DOCK

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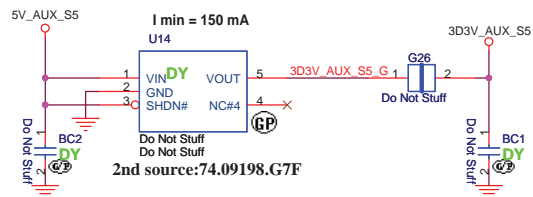
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Size: A3 Document Number: **Olan** Rev: **SA**

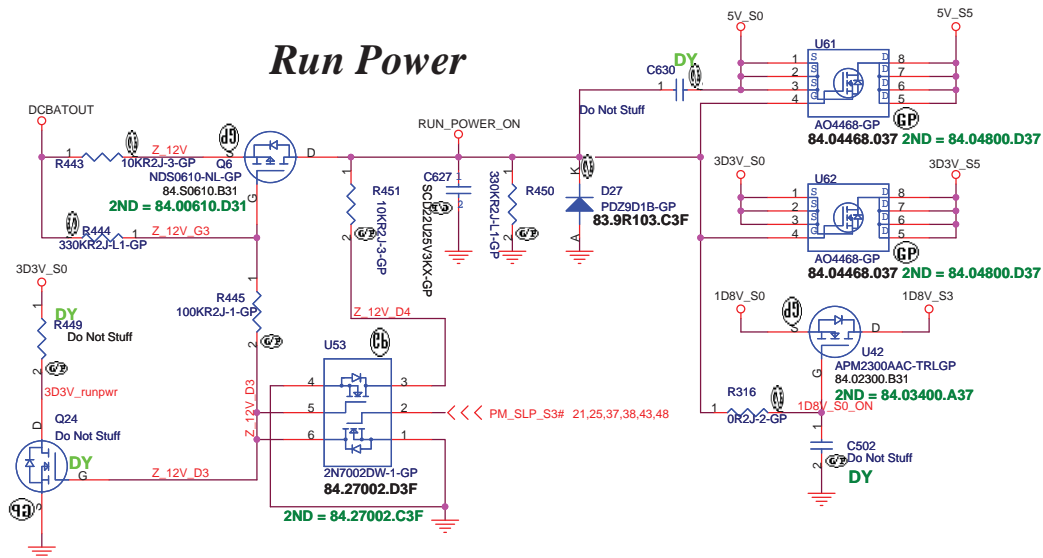
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Aux Power 3D3V_AUX_S5



Run Power

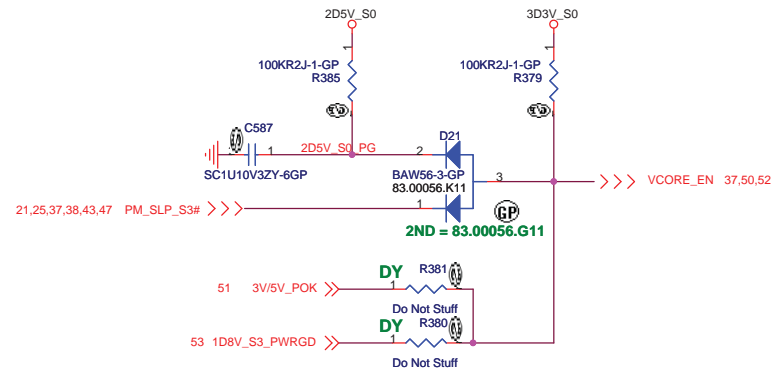


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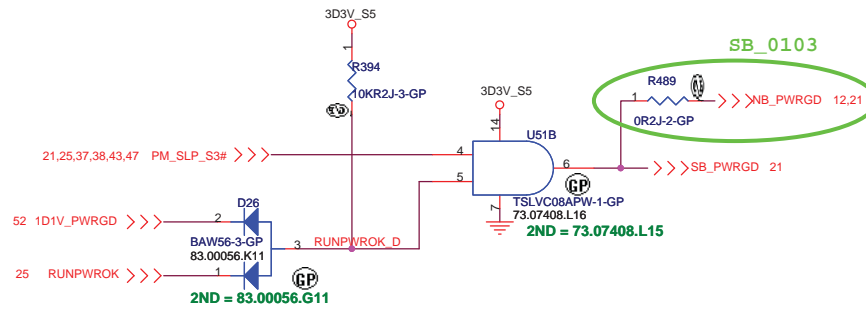
緯創資通 **Wistron Corporation**
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Title	<i>RUN POWER and 3D3V_AUX_S5</i>
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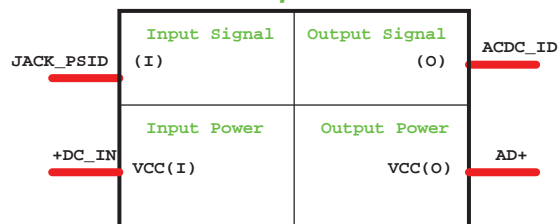


P/H @ 1D8V_S3 PAGE

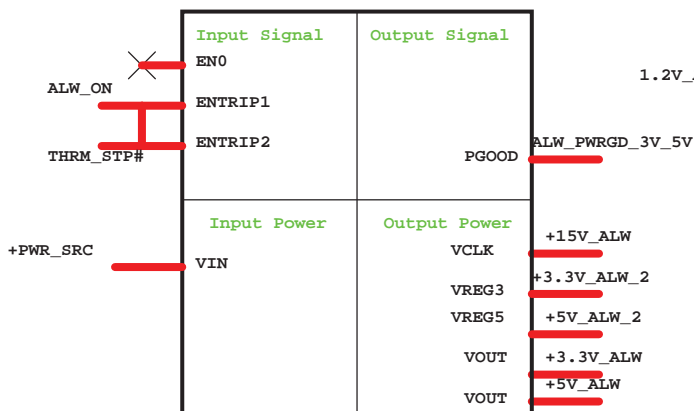


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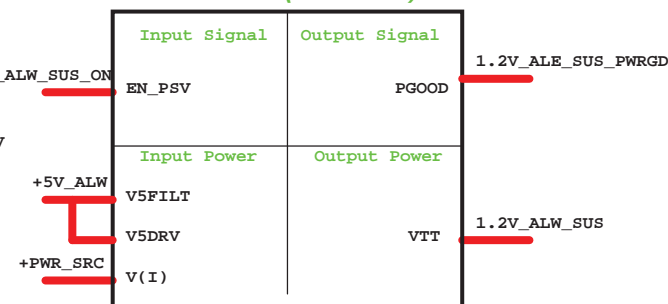
Adapter



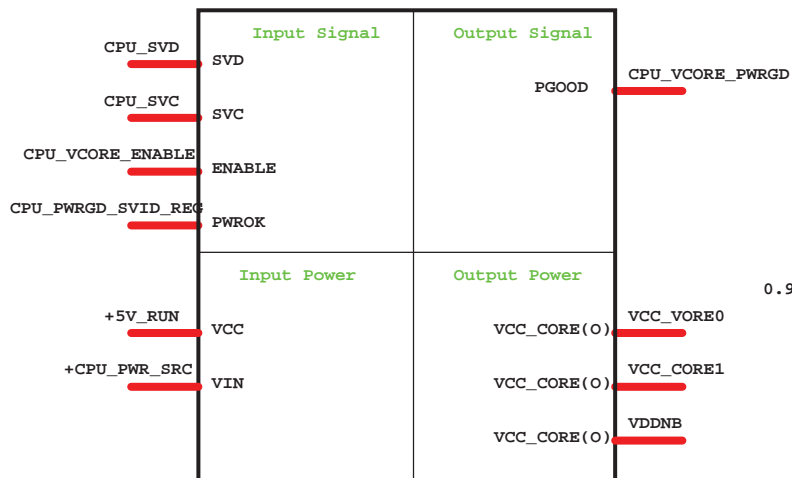
SN0608098



DCDC 1D2V(TPS5117)

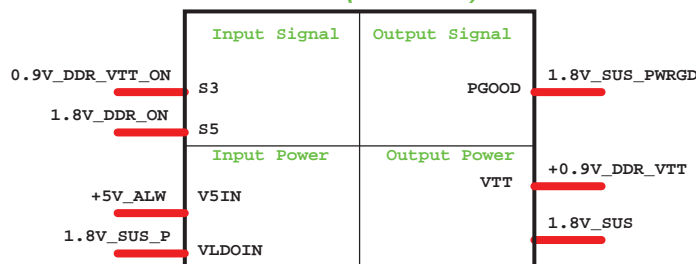


CPU_CORE ISL6265HRTZ

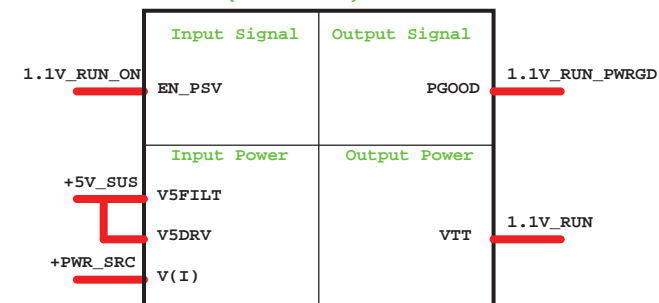


	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	1	1	1
S4	0	0	0	0	0

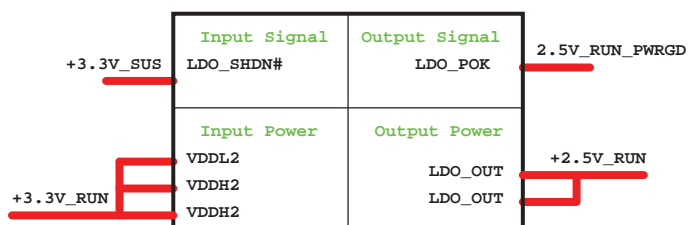
1D8V/0D9V(TPS5116)



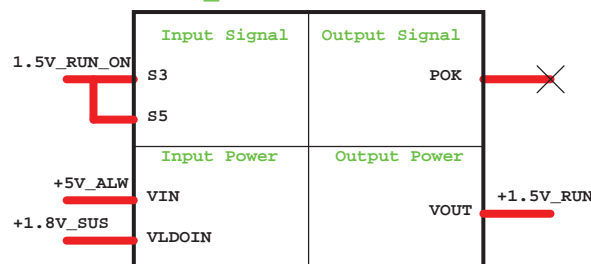
1D1V(TPS5117)



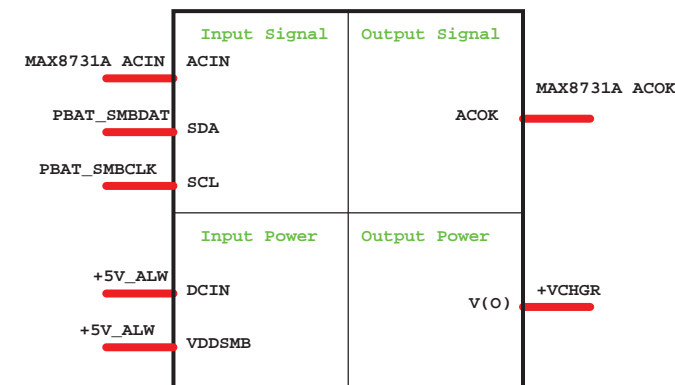
2.5V LDO EMC4002



1.5V LDO



CHARGER BQ24745



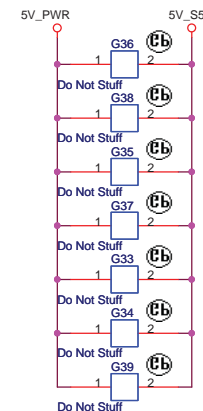
DIS DOCK

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Title Power Block Diagram

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DCBATOUT 51125

11/2

C624 C349 C626 Do Not Sit DY C625

SC10U23B50XK-1GP

5 4 3 2 1

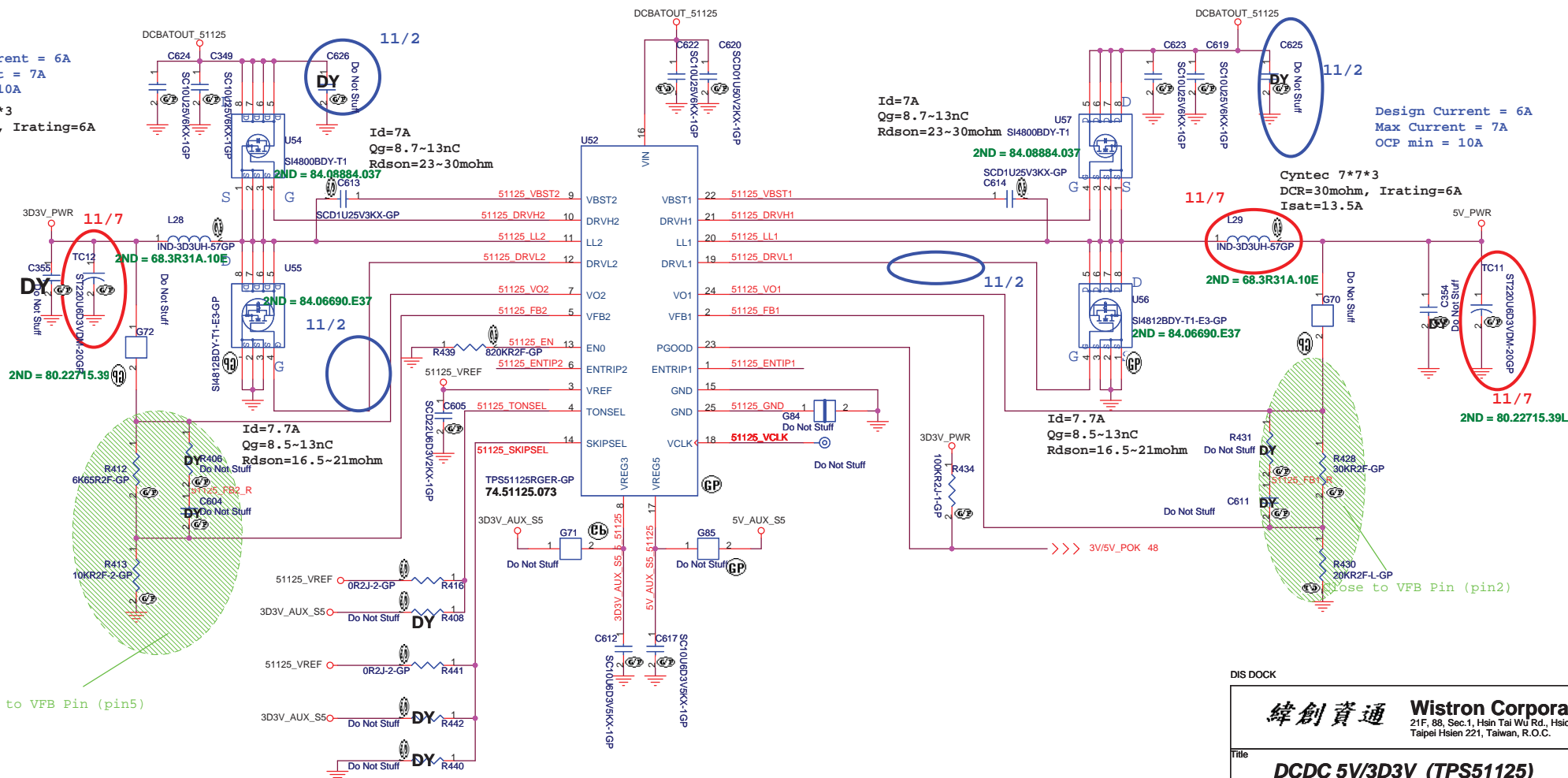
U54

SI4800BDY-T1

Id=7A
Qg=8.7~13nC
Rds(on)=23~30mohm

Id=7A
Qg=8.7~13nC
Rdson=23~30

Design Current = 6A
Max Current = 7A
OCP min = 10A



Close to VFB Pin (pin5)

DIS DOCK

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Title

DCDC 5V/3D3V (TPS51125)

Size

Document Number

Olan

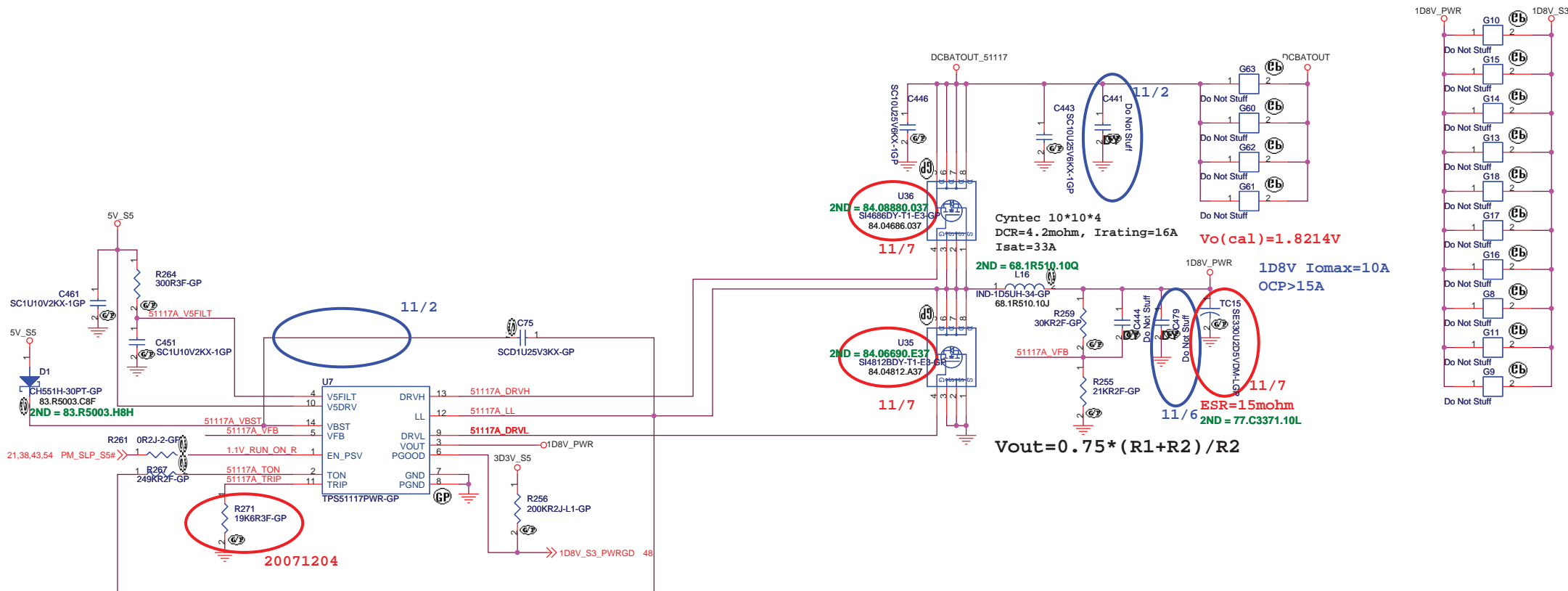
Rev

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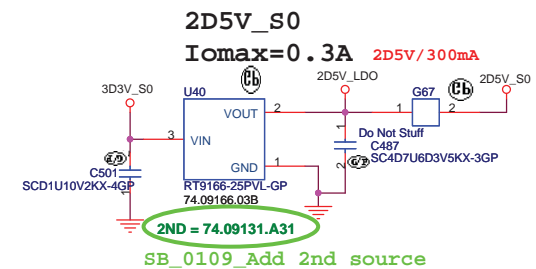
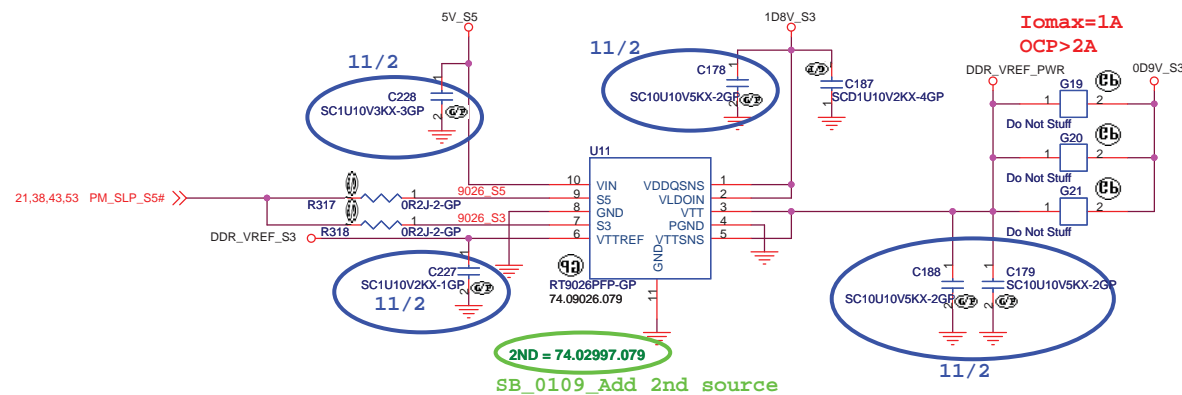
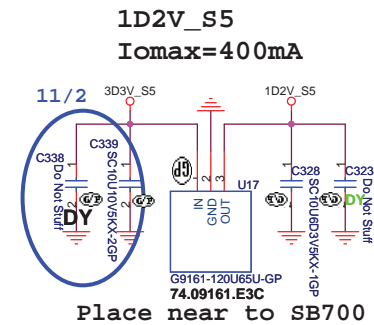
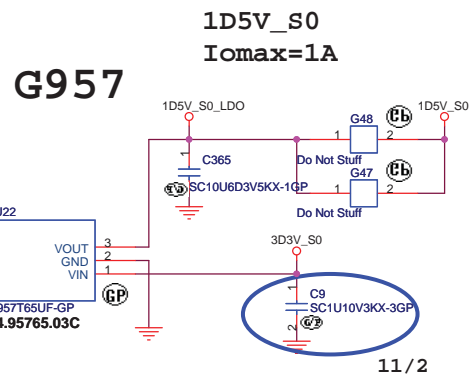
5



DIS DOCK

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Title			1D8V(TPS5117)
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DIS DOCK

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Title
0D9V&2D5V&1D25V&1D5V

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Olan

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Rev
SA



Adaptor in to generate DCBATOUT

AD_DOCK

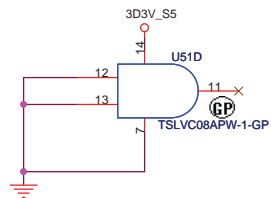


BATTERY CONNECTOR

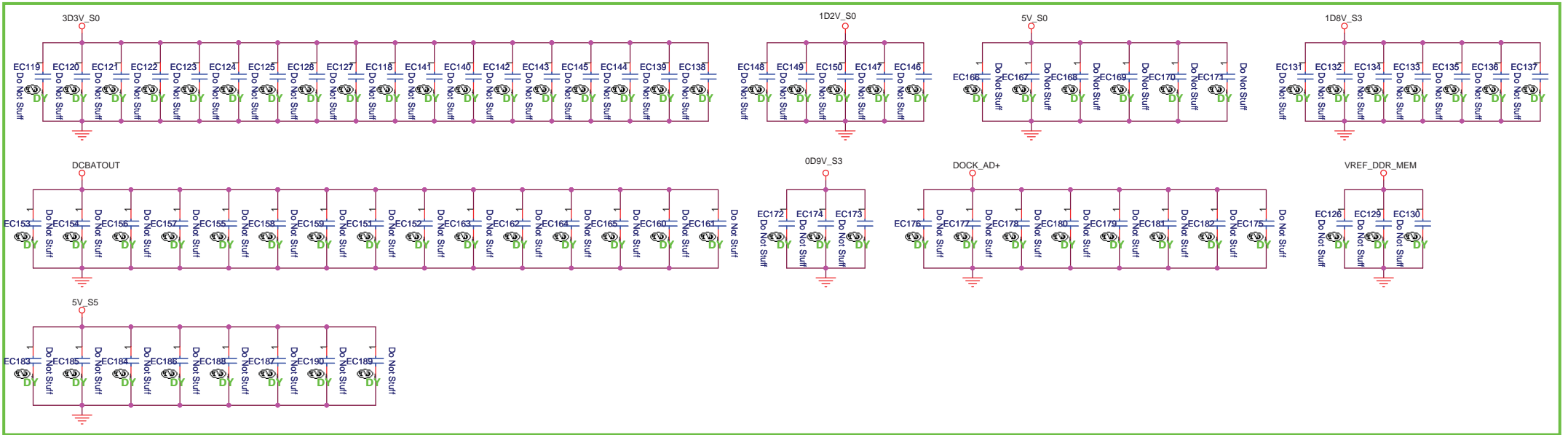


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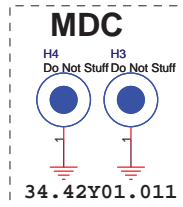
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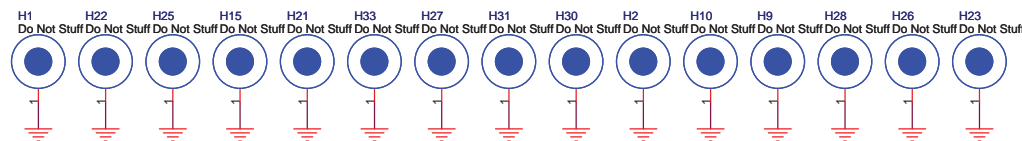
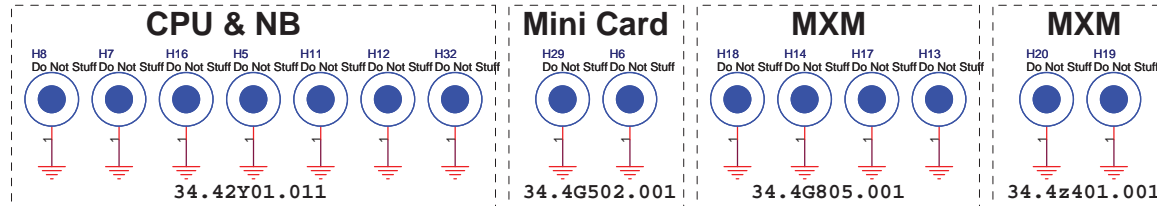
SB



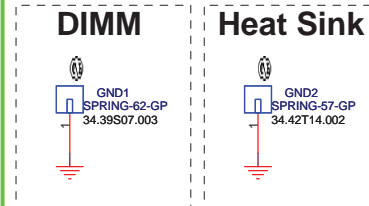
STAND OFF ON TOP



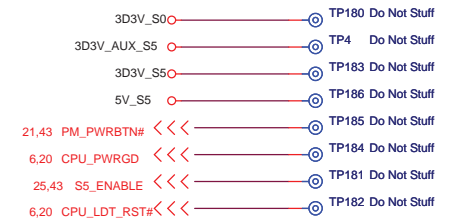
STAND OFF ON BOTTOM



SPRING ON BOTTOM



Check test point



Test Point放在Dimm Door打開可量測處

DIS DOCK

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Title		
EMI/Spring/Boss		
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